ARMY TM 11-5895-797-14

NAVY NAVELEX 0967-LP-547-0010

AIR FORCE TO 31R5-2G-101

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT, AND GENERAL SUPPORT MAINTENANCE MANUAL

ANALOG-DIGITAL CONVERTER CV-3034A/G (NSN 5805-01-018-4668)

DEPARTMENTS OF THE ARMY, THE NAVY, AND THE AIR FORCE

MARCH 1977

WARNINGS

Operator and maintenance personnel should be familiar with the safety requirements before attempting installation or operation of the equipment covered by this manual. Failure to follow requirements and observe safety precautions could result in injury or DEATH.

HIGH VOLTAGE is used in this equipment. DEATH ON CONTACT may result if safety precautions are not observed. DANGEROUS VOLTAGES EXIST IN THE FOLLOWING AREAS:

Front panel fuse terminals Front panel POWER switch Rear panel power connector Center panel power transformer line filter terminals	120 volts

NEVER should any personnel reach within or enter an equipment enclosure to service or adjust the equipment without the presence or assistance of another person capable of rendering aid.

Do not operate the equipment without a suitable ground connection. Electrical defects in the unit, loadlines, or load equipment can cause DEATH by electrocution when contact is made with ungrounded system.

TECHNICAL MANUAL
No. 11-5895-797-14
TECHNICAL MANUAL
NAVELEX 0967-LP-547-0010
TECHNICAL ORDER
TO 31R5-2G-101

DEPARTMENTS OF THE ARMY, THE NAVY,

AND THE AIR FORCE

WASHINGTON, DC, *11 March 1977*

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REPORTING OF ERRORS

You can improve this manual by recommending improvements using DA Form 2028-2 (Test) located in the back of the manual. Simply tear out the self-addressed form, fill it out as shown on the sample, fold it where shown, and drop it in the mail.

If there are no blank DA Forms 2028-2 (Test) in the back of your manual, use the standard DA Form 2028 (Recommended Changes to Publications and Blank Forms) and forward to the Commander, US Army Electronics Command, ATTN: DRSEL-MA-Q, Fort Monmouth, NJ 07703.

For Air Force, use USAFLC Form 252 (Request for TO Revision or Change). Forward direct to prime ALC/ MST. Revision or Change). Forward direct to prime ALC/ MST.

For Navy, mail comments direct to Commander, Naval Electronics Systems Command, Code 4903, Washington, DC 20360.

In each case, a reply will be furnished direct to you.

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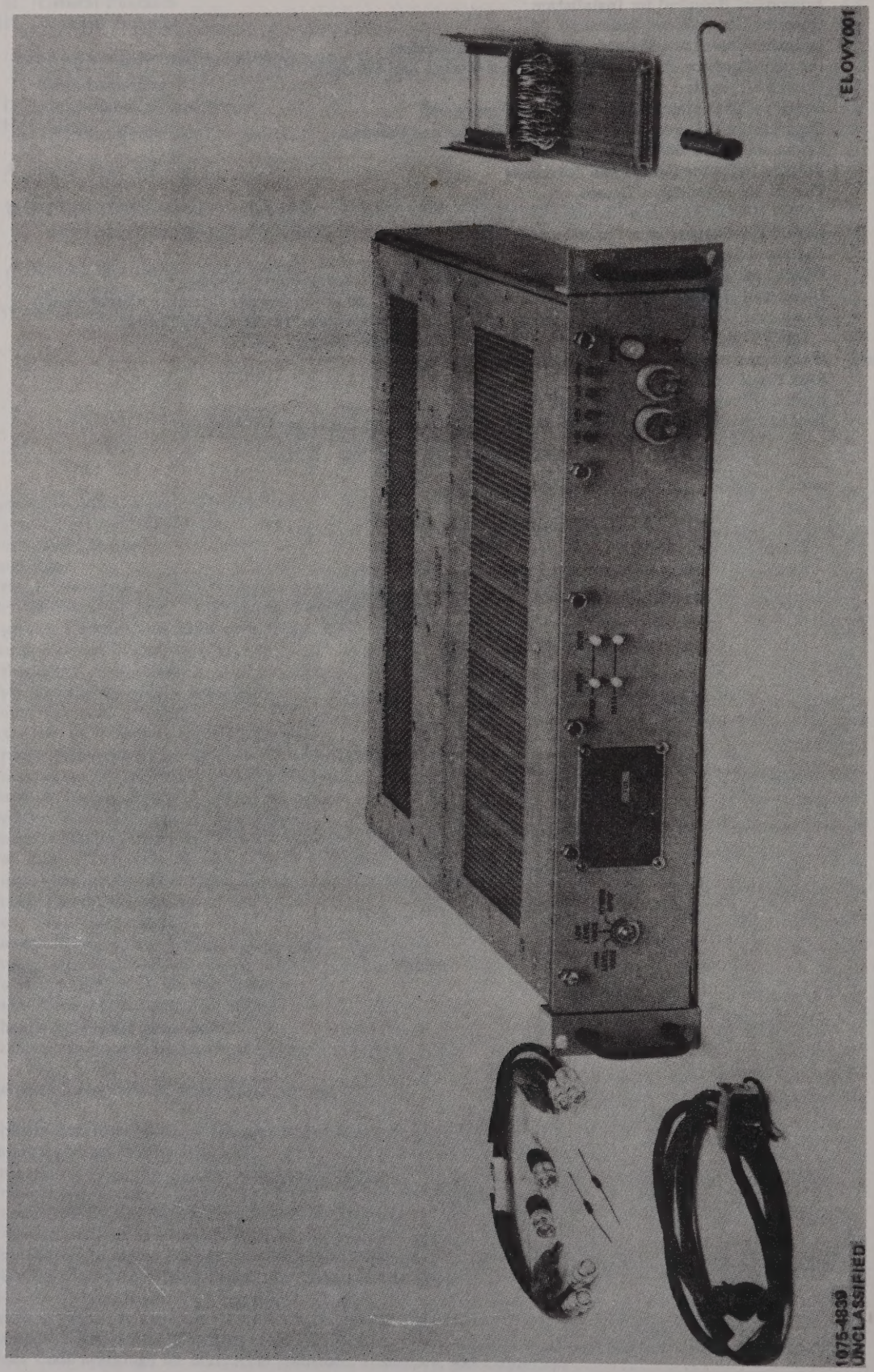


Figure 1-1. Analog-Digital Converter CV-3034A/G.

CHAPTER 1

INTRODUCTION

Section I. GENERAL

1-1. Scope

a. This manual describes Analog-Digital Converter CV-3034A/G (fig. 1-1), hereinafter called the converter. The manual contains instructions for installing, operating and maintaining the converter at operator, organizational, general support, and direct support maintenance. Appendix A contains a list of current publications applicable to the converter. Maintenance responsibilities are allocated to operating and maintenance personnel as directed in the maintenance allocation chart (MAC), appendix C.

b. TM 11-5895-797-24P contains repair parts information for maintenance categories covered in this manual and the depot maintenance work requirements (DMWR) manual.

c. The depot maintenance work requirements manual (ECOMDMWR 11-5895-797) contains information for troubleshooting individual printed wiring boards with the aid of test fixtures as well as with the converter. The maintenance section consists of depot maintenance information for repairing the converter chassis, and replacement of discrete components on the chassis and on the printed wiring boards.

1-2. Indexes of Publications

a. DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA PAM 310-7. Refer to DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

1-3. Forms and Records

a. Reports of Maintenance and Unsatisfactory Equipment. Maintenance forms, records, and reports which are to be used by maintenance personnel at all maintenance levels are listed in and prescribed by TM 38-750 (Army). Air Force personnel will use AFM 66-1 for maintenance reporting and TO-00-35D54 for unsatisfactory equipment reporting. Navy personnel will report maintenance performed utilizing the Maintenance Data Collection Subsystem (MDCS) in accordance with OPNAVINST 4790.2, Vol 3 and unsatisfactory material/conditions (UR submissions) in accordance with Vol 2, chapter 17.

b. Report of Packaging and Handling Deficiencies. Fill out and forward DD Form 6 (Packaging Improvement Report) as prescribed in AR 700-58/NAVSUPINST 4030.29/AFR 71-13/MCO P4030.29A, and DSAR 4145.8.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33A/AFR 75-18/MCO P4610.19B and DSAR 4500.15.

1-4. Destruction of Army Electronics Materiel

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

1-5. Administrative Storage

Administrative storage of equipment issued to and used by Army activities shall be in accordance with TM 740-90-1.

Section II. DESCRIPTION AND DATA

1-6. Purpose and Use

The converter interfaces full duplex hybrid analog-digital users with all digital interfaces of the communications subsystems of the Defense Satellite Communications System. The unit may service a single channel user having a contingency link terminal, or be multiplexed with other channels working into a high capacity terminal or an interconnect facility.

1-7. Description

a. The converter is an all-metal unit designed for installation in a standard 19-inch relay rack, if required. The transmitter section of the converter converts analog (voiceband) signals to digital output, and the receiver converts digital signals to analog output. Each section can operate independently of the other.

b. All operating controls and indicators are located on the front panel together with two fuses which are mounted in blown-fuse indicating fuseholders. Components of the power supply are mounted on the center panel, which becomes accessible by removal of the converter rear top cover. The 120 vac input is located on the rear panel, and all other connections are made through rear panel connectors.

1-8. Items Comprising an Operable Equipment

Analog-Digital Converter CV-3034A/G and power cable comprise an operable equipment.

1-9. System Application

The converter is designed to permit transmission over a communication link in a digital form, whether the original input is analog (voice) or digital. Refer to systems planning section, chapter 2, section I, for details.

1-10. Tabulated Data

a. Dimensions and Weight.

Height	3½ in.
Depth	19 in.
Width	17¼ in., exclusive of mounting brackets at front, for mounting in a standard 19-inch relay rack.
Weight	19 lb.

b. Technical Characteristics.

Power requirements:	
Type	120±12 vac, 45—420 Hz, single phase
Consumption	30 watts.
Temperature:	
Nonoperating	−54 to +68° C.
Operating	0 to +50° C.
Transmitter:	
Input voice Mode	Nominal 3 kHz voiceband signal
Signal level	−46 to −16 dbm (low level) or −30 to 0 dbm (high level)
Input impedance	600 ohms, balanced
Input hybrid mode	Voice and 50 kbps data signal
Voice signal level	−30 to 0 dbm
Data signal level	−15 to 0 dbm
Input impedance	135 ohms, balanced
Transmitter clock	Free run with voice signal input. Locked to data signal frequency with data signal input
Frequency	7,200,000±200 Hz
Stability	±60 ppm in free run
Tracking range	±500 ppm (±3600 Hz) with data input
Clock output	50,000 Hz squarewave
Signal level	±3 volts bipolar
Impedance	75 ohms, balanced
Transmitter output	50 kbps digital signal
Output 1:	
Signal level	±3 volts bipolar
Impedance	75 ohms, balanced
Output 2:	
Signal level	0±1 dbm
Impedance	135 ohms balanced or unbalanced.
Recevier:	
Input signal	50 kbps ditigal signal
Input 1:	
Signal level	±3 volts bipolar, minimum acceptable ±0.1 volts
Impedance	75 ohms, balanced
Input 2:	
Signal level	0 dbm nominal, minimum acceptable −15 dbm.
Impedance	135 ohms balanced or unbalanced
Receiver clock	Locked to incoming digital data signal or lock to external clock
Frequency	7,200,000 ±200 Hz
Stability	Equal to stability of locking frequency
Tracking range	±500 ppm (±3600 Hz)
External clock input	50,000 Hz squarewave
Signal level	±3 volts bipolar, minimum acceptable ±0.1volts
Impedance	75 ohms, balanced.
Output voice mode	Nominal 3 kHz voiceband signal
Signal level	−30 to 0 dbm (low level) or −23 to +7 dbm (high level); each continuously adjustable over +2 to −8 db range*
Output impedance	600 ohms, balanced
Output hybrid mode	Voice and 50 kbps data signal
Voice signal level	−30 to 0 dbm; continuously adjustable over +2 to −8 db range*
Data signal level	0 ±1 dbm
Output impedance	135 ohms, balanced.

*Adjustment control is located inside equipment and is factory set.

CHAPTER 2

SERVICE UPON RECEIPT AND INSTALLATION

Section I. SERVICE UPON RECEIPT

2-1. General

a. For digital applications, the converter typically interfaces with a time division multiplexer (TDM) (such as the AN/GSC-24), a phase shift keying (PSK) or interconnect facility (ICF) modulator-demodulator (modem) (fig. 2-1). The TDM and the modems in a typical installation have a balanced, low-level digital interface compatible with the converter. The transmitter section of the converter provides data and clock outputs. In most cases, data and clock inputs are provided to the receiver section of the converter. However, if a clock input is not provided, the timing unit can be strapped (para 2-7) to derive clock signals from the received data.

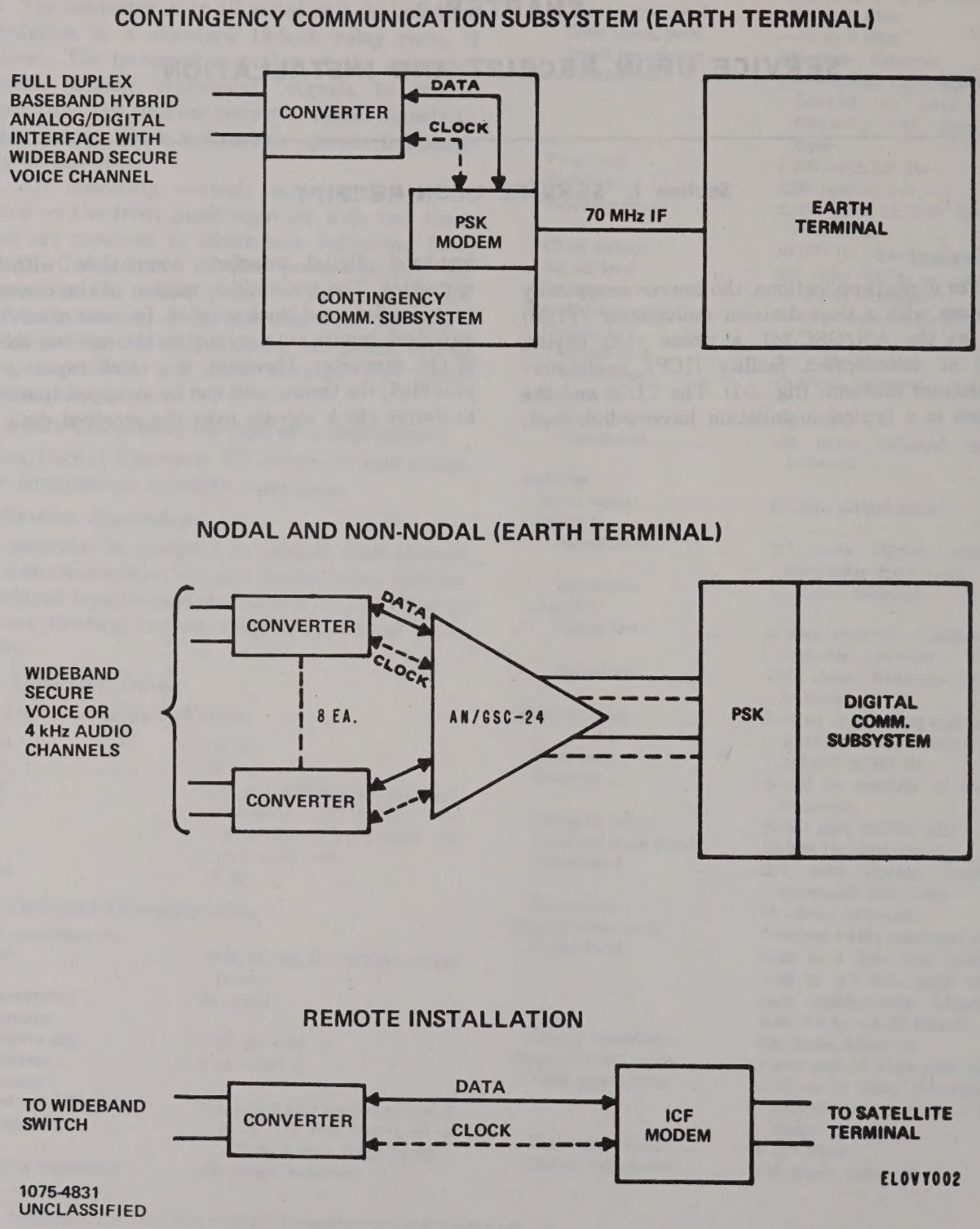


Figure 2-1. Typical system installations.

b. On the user side, signal sources may be 4 kHz audio channel from a frequency division multiplexer (FDM) or hybrid signals from a wideband switch or a wide and secure device. The audio channel carries a voiceband (analog) signal limited to 3 kHz bandwidth. If the user is a hybrid device, the transmitter determines if the signal is analog or digital and processes it accordingly. Also, the receiver deter-

mines automatically if input is of analog or digital origin. The only transmitter input on the user side is the input signal. No clock is required at this interface.

2-2. Unpacking
(fig. 2-2)

The procedures for unpacking the equipment are standard. Proceed as follows:

a. Remove the tape sealing the shipping container.

b. Remove the cushioning pads on the handles of the equipment.

c. Using the handles, lift the converter out of the container.

d. Lift out the cushioning pads at the sides of the container and remove maintenance manuals, power cable, test accessories kit, and extender boards (note that one of the extender boards contains a board extractor).

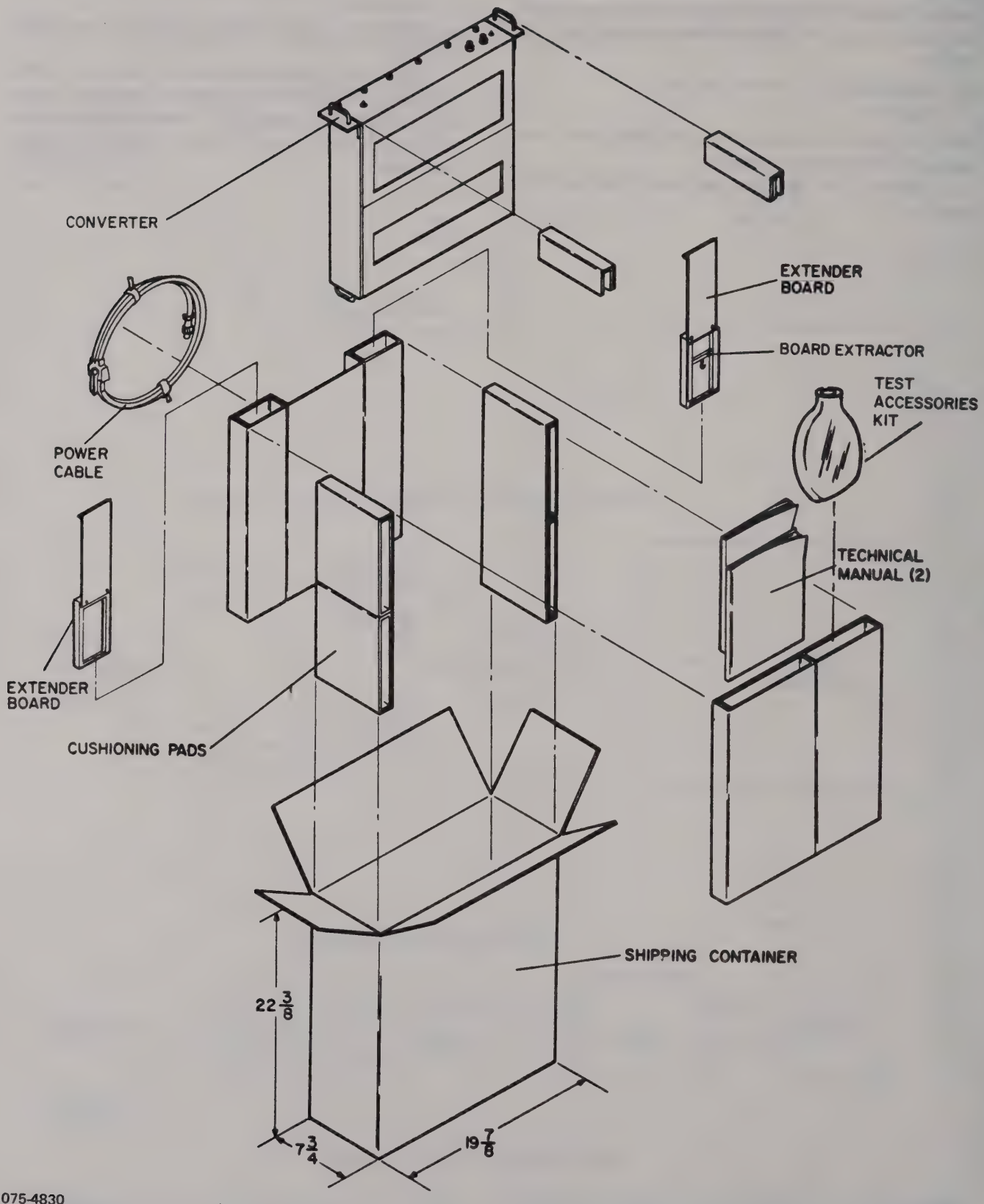


Figure 2-2. Packaging diagram.

2-3. Checking Unpacked Equipment

a. Inspect the equipment for damage incurred during shipment. If the equipment has been damaged report the damage on DD Form 6 (para 1-3b).

b. Check the equipment against the enclosed packing slip and table 2-1. Report all discrepancies in accordance with paragraph 1-3*b*. The equipment should be placed in service even though a minor assembly or part that does not affect proper functioning is missing.

Table 2-1. Components in Shipping Container

Qty	Component	Part number		Dimensions (in). Height	Width	Depth	Wt (lb)
1	Analog-Digital Converter CV-3034A/G	SMD865116	(80063)	3-1/2	18	19-3/4	19
2	Extender Board	SMD750075	(80063)	3-1/8	1-1/8	15	1/2
1	Board Extractor	SMC750009	(80063)	3	1/2	3	1/4
1	Power Cable	SMD750076	(80063)			10 ft	1/2
1	Test Accessories Kit	SMD865106	(80063)				1/2
2	Technical Manuals: TM 11-5895-797-14						

c. Check to see if the equipment has been modified. (Equipment that has been modified will have the modification work order (MWO) number on the front panel, near the nomenclature plate.) Check to see whether all currently applicable MWO's have been applied. (Current MWO's applicable to the equipment are listed in DA PAM 310-7.)

d. For dimensions, weights, and volume of packaged items, refer to SB 700-20.

2-4. Packaging

Procedures for packaging the equipment for shipment or limited storage depend on the material available and the conditions under which the material is to be packaged or stored. In general, the packaging procedure is as follows:

a. Place the board extractor in one of the extender boards.

b. Place the cushioning pads at the sides of the container.

c. Insert the manuals, power cable, test accessories kit, and extender boards into the cushioning pads.

d. Insert the converter into shipping container so that the handle flanges are supported on top of the cushioning pads, and include desiccant.

e. Close the container and secure the top with sealing tape.

Section II. INSTALLATION INSTRUCTIONS

NOTE

The following installation procedures require the assistance of direct support or higher category maintenance personnel.

2-5. Test Equipment Required for Installation

Table 2-2 lists the equipment required for performing installation checks. Jumper cable and terminator details are provided in TM 11-5895-797-24P.

2-6. Installation Instructions

Mount the converter in a standard 19-inch rack adjacent to the equipment using the converter. All external connections are made at the rear panel (fig. 2-3).

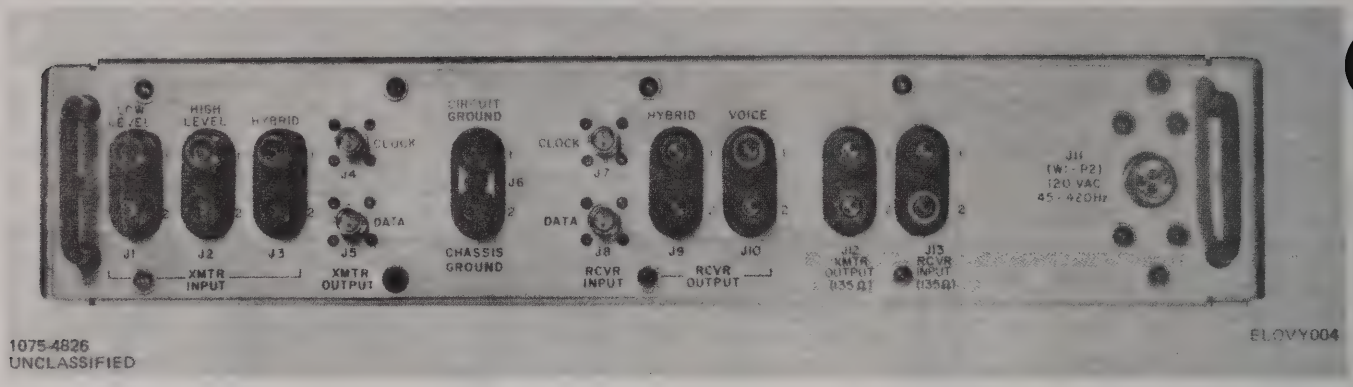


Figure 2-3. Rear panel.

2-7. Special Installations

Details of the electrical installation vary with the system with which the converter is used. The following procedures are required for correct electrical installation and depend on associated equipments.

a. When input and output data signals require positive or negative biasing to offset potentials between associated equipments, remove the shorting link of connector J6 on the rear panel. Connect the required offset bias from an external power supply between CIRCUIT GROUND and CHASSIS GROUND of connector J6.

Table 2-2. Equipment Required for Installation

Item	Designation[a]	Purpose	Applicable publication
Counter, Electronic, Digital	CP-727/U	To measure clock frequency.	TM 11-6625-1548-15
Audio Signal Generator	SG-632/U	To supply test signals.	TM 11-6625-1589-15 and -15-1
Wide Range Oscillator	O-1025/U		TM 11-6625-1537-15
Oscilloscope	AN/USM-273	To display waveforms for examination and comparison.	TM 11-6625-1541-15
Multimeter	AN/PSM-6B or AN/USM-210	For dc voltage and continuity testing.	TM 11-6625-475-10, -25
Oscilloscope			TM 11-6625-1722-15
Test accessories kit	Part No. SMB865106 (80063)	To test converter.	
Consisting of:			
Two test cables	Part No. SMD865108 (80063)	To connect transmitter clock and data outputs to corresponding receiver inputs.	
One test cable	Part No. SMC865154 (80063)	To connect transmitter 135 ohm output to receiver 135 ohm input.	
Two terminators	Part No. SMC865134 (80063)	Dummy load for transmitter outputs.	
Resistor, 620 ohm, ±5%, ½ watt.	RCR20G621J	Dummy load for voice terminal.	
Resistor, 130 ohm, ±5%, ½ watt.	RCR20G131J	Dummy load for hybrid terminal.	
Extender Board[b]	Part No. SMD750075 (80063)	For fault isolation of discrete components on printed wiring boards.	
Board Extractor[b]	Part No. SMC750009 (80063)	For removal of printed wiring board.	

[a] Or equivalent.
[b] Supplies with each converter.

b. When the equipment is shipped, the voiceband output of the receiver is strapped for low level (0 dbm). If high level voiceband (+7 dbm) is required, strap the terminals on printed wiring board 1A9 in accordance with instructions in paragraph 2-10*c*.

c. When the equipment is shipped, the receiver timing is strapped for use with an external clock. If an external clock input to the receiver is not available, strap the terminals on printed wiring board 1A7 in accordance with instructions in paragraph 2-10*d*.

2-8. Interconnections and Cabling

a. Connect the power cable to J11 (W1-P2) on the rear panel (fig. 2-3). Plug the other end of the cable to a 120 vac, 45-420 Hz, standard power receptacle.

b. Make the following interconnections to rear panel connectors as required by the overall system plan at the completion of preliminary checks and adjustments (para 2-9).

(1) If user is a hybrid circuit, connect input signal source to HYBRID XMTR INPUT J3.

(2) If user is an analog voice circuit, connect signal source to LOW LEVEL XMTR INPUT J1 or HIGH LEVEL XMTR INPUT J2 as required.

(3) The XMTR OUTPUT DATA connector J5 is a balanced digital signal and is connected to a digital multiplexer or modem.

(4) The RCVR INPUT DATA at connector J8 is a balanced digital signal from a digital multiplexer or modem.

(5) The XMTR OUTPUT CLOCK at connector J4 accompanies the signal to the demultiplexer or modem.

(6) The RCVR INPUT CLOCK at connector J7 comes with the receiver input signal from the demultiplexer or modem, except when the receiver is operating from signal derived timing. (Refer to paragraphs 2-7*c* and 2-10*d*.)

(7) The HYBRID RCVR OUTPUT at connector J9 is connected to the user, when required for a hybrid circuit.

(8) The VOICE RCVR OUTPUT at connector J10 is connected to the user when required for an analog voiceband circuit.

(9) The XMTR OUTPUT (135 Ω) at connector J12 is a transformer-coupled, balanced digital signal at a 50 Kbps rate, and is to be connected to a digital multiplexer or modem.

NOTE

Only RCVR INPUT DATA ((4) above, or RCVR INPUT (135 Ω) ((10) below) should be used at one time. Attempting to use both inputs simultaneously will result in erroneous reception.

(11) The RCVR INPUT (135 Ω) at connector J13 is a transformer-coupled, balanced 135 ohm input which should be connected to the 50 Kbps digital bit stream from a demultiplexer or modem.

NOTE

Refer to paragraph 2-7*a* for signal ground biasing. If necessary remove link from rear panel connector J6 and connect the proper direct current biasing voltage supply.

Section III. PRELIMINARY ADJUSTMENT OF EQUIPMENT

2-9. Preliminary Checks and Adjustment

Because critical adjustments can be affected during shipment of the converter, perform procedures listed in paragraph 3-3, then perform procedures in paragraphs 5-8*b*, 7-8 and 7-9. If malfunctions occur during test, refer to troubleshooting table 5-3, 7-2, 7-3, or 7-4, as necessary.

2-10. System Lineup.

The equipment is shipped ready for operation in most installations. Exceptions require modification of terminal strapping on printed wiring boards 1A7 and 1A9. If the system plan requires changes to be made, proceed as follows:

a. Loosen the six captive screws and open the front panel.

b. Insert the board extractor into the hole of the applicable printed wiring board and withdraw 1A7 and 1A9, or both, as the modification requires.

NOTE

A short piece of No. 24 wire is used for the strapping, and a soldering iron is required to make the connection.

c. For normal operations or low level voiceband output at the receiver, terminals E1 and E2 of printed wiring board 1A9 (fig. 2-4) are strapped together. If high level voiceband output at the receiver is required, remove the strap between terminals E1 and E2 and solder strap terminal E1 to E3. In addition to the strapping, the output level can be continuously adjusted over a range of +2 to −8 db by variable resistor R15 (fig. 2-4). Resistor R15 is factory-set, and adjustment is normally not required. If adjustment of R15 is required, perform voice throughput check (para 7-9*a*).

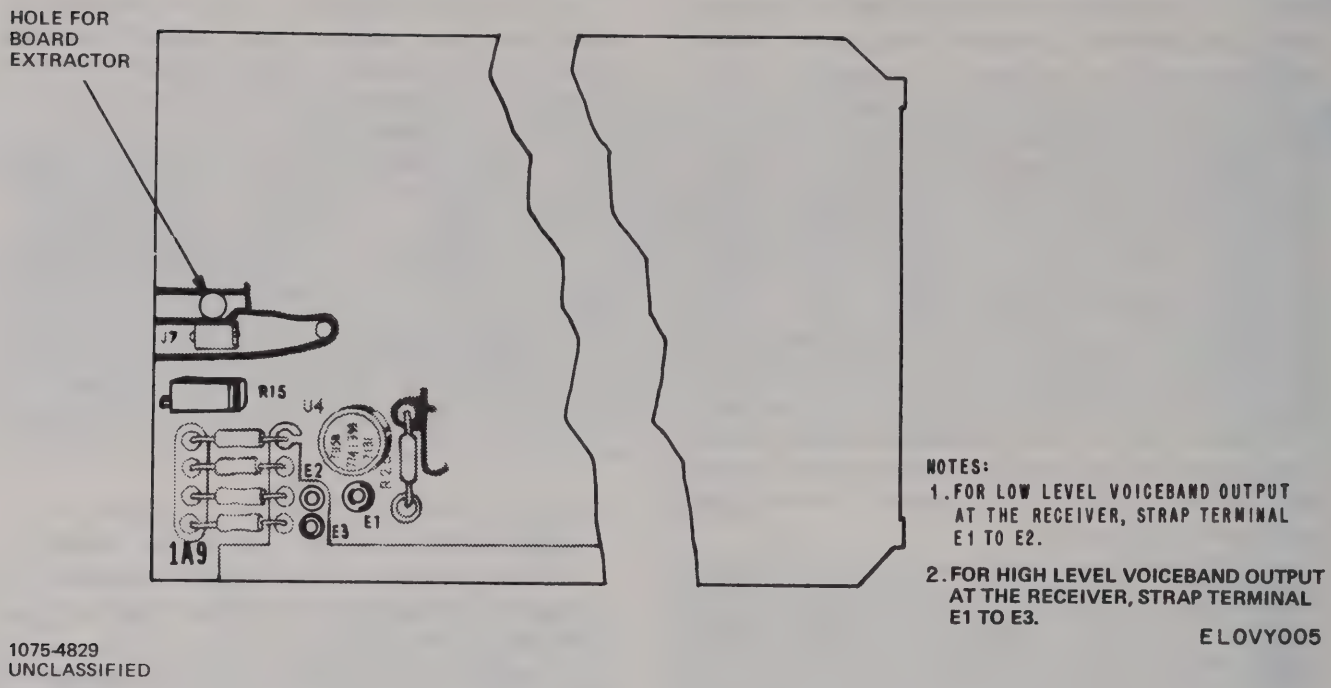


Figure 2-4. Printed wiring board 1A9 strapping terminals E1, E2, and E3.

d. If timing signals are to be received from an external clock, terminals E1 and E2 of printed wiring board 1A7 (fig. 2-5) are strapped together. This is the normal operation. If the receiver timing signal must be derived from the internal clock slaved to the input signal, remove the strap between terminals E1 and E2 and strap terminal E2 to E3.

NOTE

A short piece of No. 24 wire is used for the strapping, and a soldering iron is required to make the connection.

e. Replace the printed wiring boards carefully and press them firmly and fully into place.

f. Close the front panel and tighten the six captive screws.

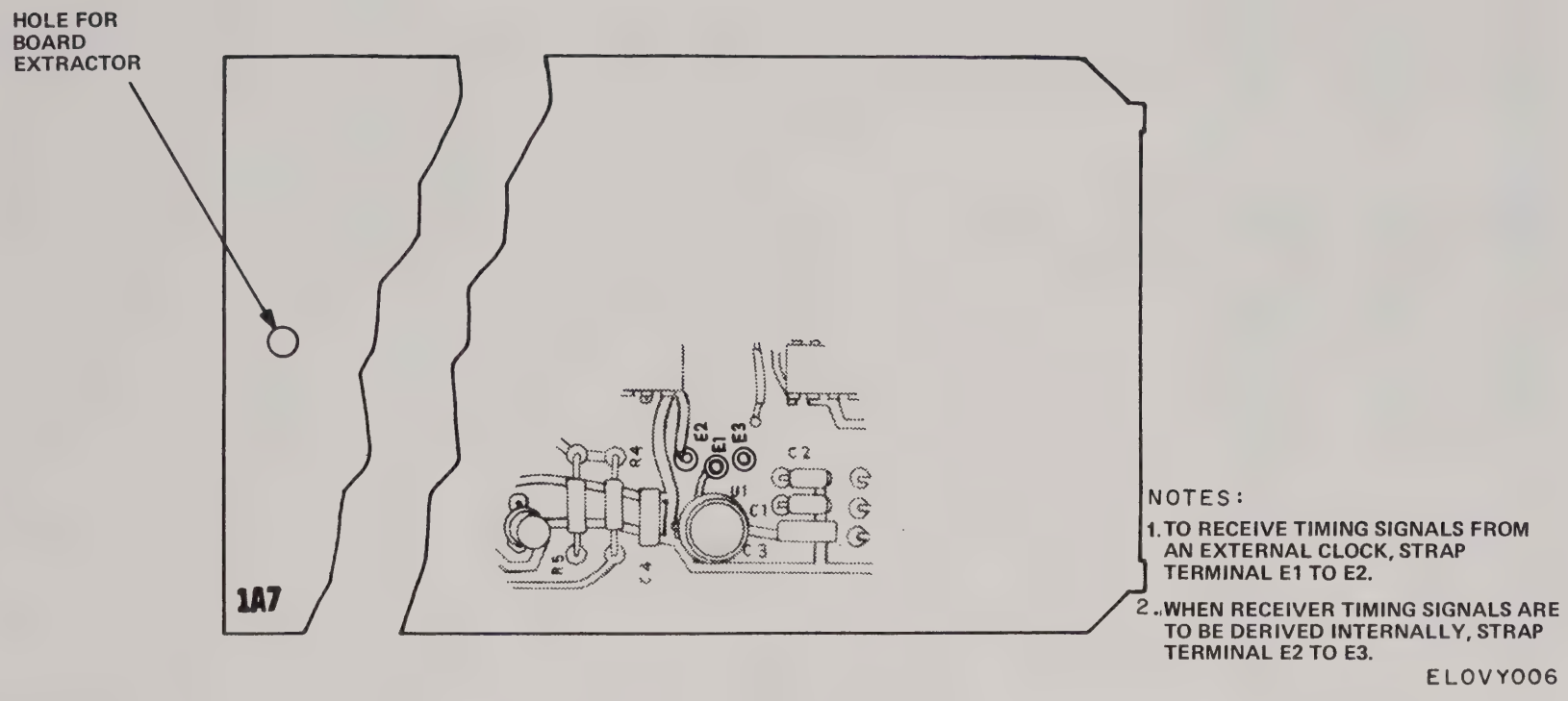


Figure 2-5. Printed wiring board 1A7 strapping terminals E1, E2, and E3.

CHAPTER 3

OPERATING INSTRUCTIONS

Section I. CONTROLS AND INSTRUMENTS

3-1. Damage From Improper Settings

No possible combination of control settings will cause damage to the equipment or create a hazard to personnel.

3-2. Operator Controls

The operator controls are listed in table 3-1 and illustrated in figure 3-1.

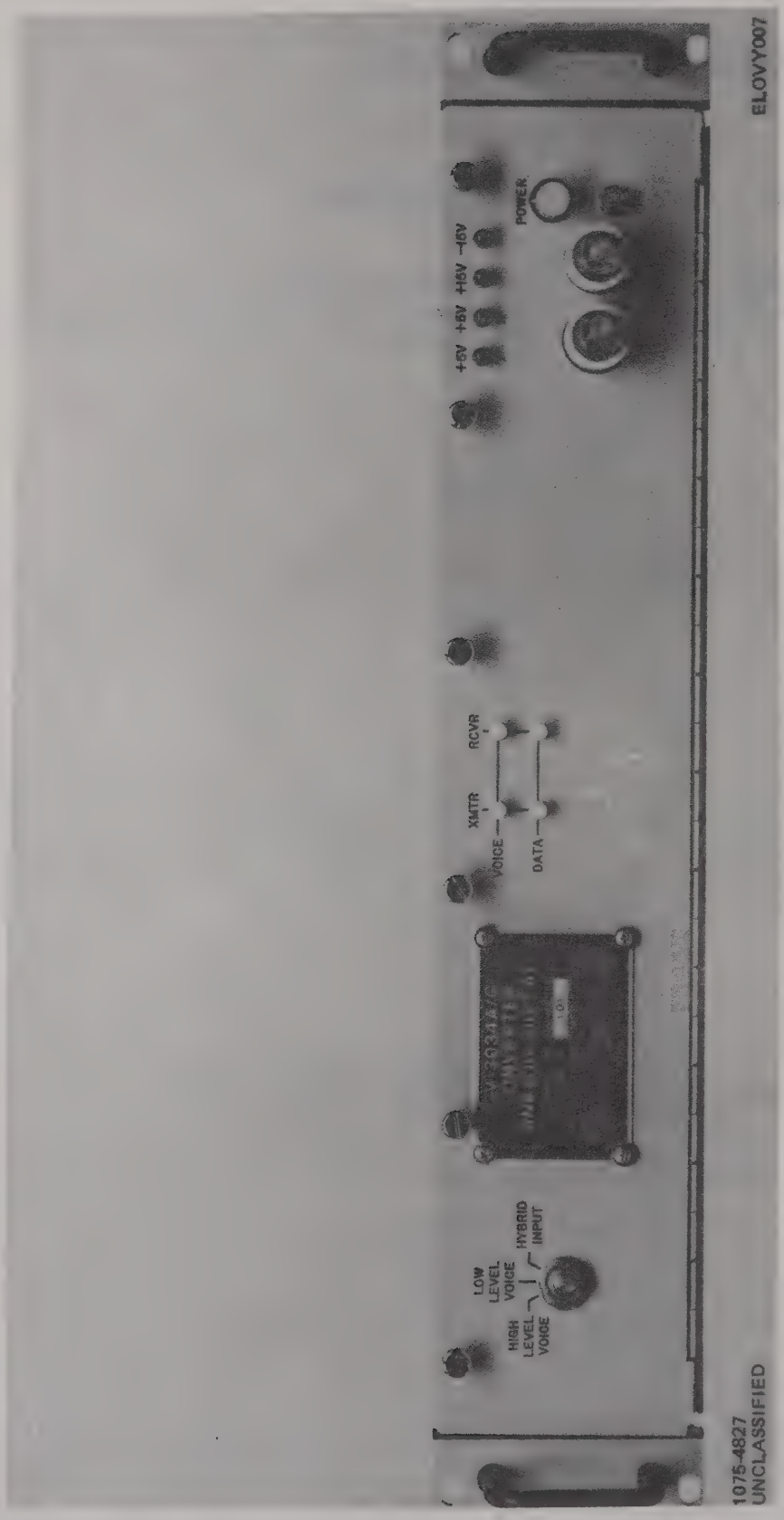


Figure 3-1. Operator controls and indicators, front panel.

Section II. OPERATION

3-3. Preliminary Starting Procedure

Before operating the equipment, the operator must perform the following:

a. Check to see that power cable is properly connected and firmly seated.

b. Set HIGH LEVEL VOICE/LOW LEVEL VOICE/HYBRID INPUT switch on front panel to desired voice position.

Table 3-1. Operator Controls and Indicators

Control, indicator, or connector	Function
HIGH LEVEL VOICE-LOW LEVEL VOICE-HYBRID INPUT (3-position screwdriver actuated) switch.	Selects one of three input signal sources. *SW pos* — *Mode* HIGH LEVEL VOICE — Selects transmitter input from HIGH LEVEL connector J2 pins 1 and 2. LOW LEVEL VOICE — Selects transmitter input from LOW LEVEL connector J1 pins 1 and 2. HYBRID INPUT — Selects transmitter input from HYBRID connector J3 pins 1 and 2.
POWER switch.	Applies or removes power to the converter.
POWER indicator lamp.	Indicates that converter is receiving power.
XMTR VOICE/DATA and RCVR VOICE/DATA yellow indicating lamps.	Indicates operating mode of transmitter and receiver.
+5V T, +5V R, +15V and −15V green indicator lamps.	Indicates that power supplies of the transmitter and receiver are operating.
Two fuses in blown-fuse indicating fuseholders.	A blown fuse causes neon lamp in fuseholder to light.

c. Place POWER switch on front panel to on position.

d. Check to see that POWER indicator lamp lights.

e. Check to see that four green voltage indicators, +5V T, +5V R, +15V and −15V, light.

f. Check to see that amber XMTR VOICE and RCVR DATA indicators light.

NOTE

During operation, only one transmitter mode lamp and one receiver mode lamp is lighted at any given time.

g. Place POWER switch in OFF position if the preliminary adjustments given in paragraph 2-9 are not performed immediately during initial start up.

3-4. Initial Adjustment

No initial adjustments are required before operating the converter.

3-5. Operating Procedure

The converter is normally in standby condition under control of associated equipment, and in the mode required by the user, after starting procedures are completed.

a. Starting Procedure. Perform procedure as follows:

(1) Insure that front panel HIGH LEVEL VOICE-LOW LEVEL VOICE-HYBRID INPUT switch is set in position required for converter operation in mode required.

(2) Place POWER switch on front panel to on position.

(3) Check to see that POWER indicator lamp lights.

(4) Check to see that four green voltage indicators, +5V T, +5 R, +15V and −15V, light.

(5) Check to see that amber XMTR VOICE and RCVR DATA indicators light.

NOTE

During operation, only one transmitter mode lamp and one receiver mode lamp is lighted at any given time.

b. Shutdown Procedure. Perform shutdown as follows:

(1) Notify associated equipment operators that converter is to be shutdown.

(2) Place POWER switch to OFF.

(3) Observe that indicators lamps are not lighted.

CHAPTER 4

OPERATOR MAINTENANCE INSTRUCTIONS

NOTE

No tools or equipment are required at the operator maintenance category.

4-1. Preventive Maintenance Checks and Services

To insure that the converter is always ready for operation, it must be inspected systematically so that defects may be discovered and corrected before they result in serious damage or failure. The necessary preventive maintenance checks and services to be performed are listed and described in tables 4-1 and 4-2. The item numbers indicate the sequence of minimum inspection requirements. Defects discovered during operation of the units will be noted for future correction to be made as soon as operation has ceased. Stop operation immediately if a deficiency is noted during operation which would damage the equipments. Record all deficiencies together with the corrective action taken on maintenance form described in TM 38-750.

Table 4-1. Operator Preventive Maintenance Checks and Services

B—Before Operation Time required: 0.5 | D—During Operation | A—After Operation Time required: 0.2

Interval and sequence No. 1			ITEM TO BE INSPECTED / PROCEDURE	Work time (M/ H)
B	D	A		
1			CLEANLINESS OF EQUIPMENT Inspect exterior surface of converter. The exterior surface should be free of dust and dirt.	0.1
2			CONTROL MARKINGS Inspect for legibility of control markings.	0.1
3			LOOSE ITEMS Gently check for loose handles and knobs. Check security of connectors by pressing in firmly.	0.1
4	1	1	OPERATING INDICATORS Check for abnormalities such as burned-out lamps and fuses. For replacement instruction refer to paragraph 5-7.	0.2

Table 4-2. Periodic Operator Preventive Maintenance Checks and Services

D—Daily Time required: 0.1 | W—Weekly Time required: 0.1

Interval and sequence No. 1		ITEM TO BE INSPECTED / PROCEDURE	Work time (M/ H)
D	W		
1		CLEANLINESS OF EQUIPMENT Inspect exterior surfaces of converter. The exterior surfaces should be free from dust and dirt. WARNING The fumes of trichloroethane are toxic. Provide thorough ventilation whenever used. DO NOT USE NEAR AN OPEN FLAME. Trichloroethane is not flammable, but exposure of the fumes to an open flame or hot metal forms highly toxic phosgene gas. Clean the exterior surfaces with a soft, clean cloth moistened (not soaked) with inhibited trichloroethane (Federal Specification O-T-620, Type I, or equivalent).	0.1
	1	LOOSE ITEMS Gently check for loose handles and knobs. Check security of connectors by pressing in firmly.	0.1

4-2. Troubleshooting Information

The converter is normally under the control of associated equipment. Evaluate information recieved from other operators in the overall communication system that could indicate malfunction of the converter. Troubleshooting at the operator category is limited to replacing the fuses and the power indicator lamp (table 4-3). Any trouble beyond the scope of the operator shall be referred to higher category maintenance.

Table 4-3. Operator Troubleshooting Chart

Malfunction	Probable cause	Corrective action
1. Power indicator lamp power supply voltage indicator (green) lamps and mode indicator (yellow) lamps are not lighted.	*a.* No primary power	*a.* Check primary power source. If power source is present as noted by associated equipment, refer to table 5-3, step 1.
	b. Blown fuses F1 and/or F2. **NOTE** A lighted neon lamp in fuse holder indicates a blown fuse.	*b.* Unscrew cap of fuseholder on front panel and replace fuse.
2. Power indicator lamp not lighted, power supply voltage indicators (green) lamps lighted, and equipment operates properly.	Defective lamp (DS1)	Unscrew plastic cover on front panel and replace lamp. If converter operates correctly and lamp still is not lighted, refer to table 5-3, step 2.
3. One or more voltage indicator lamps are not lighted, power indicator lamp is lighted, and equipment operates properly.	One or more defective lamps (DS6 through DS9).	Replace defective lamp (para 5-7*a*).
4. One or more mode indicator (yellow) lamps are not lighted. **NOTE** Only one transmitter mode and one receiver mode indicator lamp is lighted at any given time during operation of equipment.	One or more defective lamps (DS2 through DS5).	Replace defective lamp (para 5-7*b*).

4-3. Cleaning, Inspection, and Repair Instructions

a. Cleaning. At the operator/crew maintenance, cleaning is limited to exterior surfaces only. Refer to table 4-1 for details.

b. Inspection. Items to be inspected before, during, and after operation, and daily and weekly checks required for the converter are listed in tables 4-1 and 4-2. Items requiring maintenance beyond the scope of the operator shall be referred to higher category maintenance.

c. Repair. Repair instructions at the operator maintenance are limited to the power indicator lamp and fuse replacement. Voltage indicator and mode indicator lamps are subminiature lamps with nonreplaceable bulbs to be replaced at higher category maintenance.

CHAPTER 5

ORGANIZATIONAL MAINTENANCE INSTRUCTIONS

Section I. GENERAL INSTRUCTIONS

5-1. Organizational Maintenance Tools and Equipment

Table 5-1 lists the tools and equipment required for maintenance of the converter at the organizational maintenance.

Table 5-1. Organizational Maintenance Tools and Equipment

Nomenclature	Designation*	Purpose	Quantity
Multimeter	AN/PSM-6B or AN/USM-210	For dc voltage and continuity checking. For wire repair and parts replacement (includes soldering iron).	1
Electronic Equipment Tool Kit	TK-105/G		1

*Or equivalent

5-2. Touchup Painting Instructions

Remove rust and corrosion from metal surfaces by lightly sanding with fine sandpaper. Brush two thin coats on the bare metal to protect it from further corrosion. Refer to the applicable cleaning and refinishing practices specified in TB 43-0118.

NOTE

The converter requires no lubrication.

5-3. Organizational Preventive Maintenance Checks and Services

To insure that the converter is always ready for operation, it must be inspected systematically so that defects may be discovered and corrected before they result in serious damage or failure. The necessary preventive maintenance checks and services to be performed are listed and described in table 5-2. The item numbers indicate the sequence of inspection requirements.

WARNING

120 vac is present at the rear panel power connector, the front panel POWER switch and fuseholder terminals. Serious INJURY or DEATH may result from contact with these points.

5-4. Troubleshooting Procedure

a. Troubleshooting at organizational consists of isolating faults in the indicator lamps, lampholder, fuseholders and associated wiring, and are given in table 5-3. To aid troubleshooting of these items, the converter interconnecting wiring diagram is provided (fig. FO-1).

b. The converter is normally under control of associated equipment; therefore, the operator's evaluation of malfunctions in the overall communication system should be considered before troubleshooting the converter. Any trouble that is beyond the scope of organizational maintenance shall be referred to higher category of maintenance.

Table 5-2. Organizational Preventive Maintenance Checks and Services

Q—Quarterly
Total man-hours required: 0.6

Sequence number	ITEM TO BE INSPECTED PROCEDURE	Work time (M/ H)
1	LOOSE ITEMS Check for tightness or firmness of rack input/output and power cable rear panel connectors, top cover screws, front panel captive screws, and rack mounting screws. Tighten as required.	0.3
2	CABLING Visually inspect cabling for fraying, chafing or other conditions that could develop into sources of trouble. Replace cables as required.	0.2
3	EXTERIOR SURFACE Check for scratches or chipped paint. For touchup instructions refer to paragraph 5-2.	01.

Table 5-3. Organizational Troubleshooting Chart

Malfunction	Probable cause	Corrective action
1. Power indicator lamp, power supply voltage indicator (green) lamps and mode indicator (yellow) lamps are not lighted (from table 4-3, step 1).	*a.* Defective fuseholders XF1 and XF2. *b.* Defective wiring to fuseholder.	*a.* Check fuseholders, replace if defective (para 5-7*c*). *b.* Check wiring to fuseholders, reconnect or replace if defective (fig. FO-1).
2. Power indicator lamp is not lighted lamp is known good, and equipment operates properly (from table 4-3, step 2).	*a.* Defective lampholder XDS1. *b.* Defective wiring to lampholder.	*a.* Check lampholder (contacts inside, solderlugs outside), replace if defective (para 5-7*c*). *b.* Check wiring to lampholders, reconnect or replace if defective (fig. FO-1).
3. Same as step 2 except equipment does not operate.	Defective cables or power supply.	Refer to table 7-2, step 1.
4. One or more power supply voltage indicator lamps are not lighted, power indicator lamp is lighted and operator has verified equipment is operating properly. Lamps are known good.	Defective wiring to lamps (DS6 through DS9).	Check wiring and reconnect or replace if defective (fig. FO-1).
5. Same as step 4 except equipment does not operate properly.	One or more power supply voltages incorrect or missing.	Perform power supply voltage check (para 5-8*b*). If incorrect or missing, perform procedures in table 7-3.
6. One or more mode indicator (yellow) lamps are not lighted and lamps are known good. NOTE Only one transmitter mode and one receiver mode indicator lamp is lighted at any given time.	Defective wiring to lamps (DS2 through DS5).	Check wiring and reconnect or replace if defective (fig. FO-1). If still defective, refer to table 7-2, step 2.

Section II. ORGANIZATIONAL MAINTENANCE OF CONVERTER

5-5. General

a. This section contains organizational maintenance procedures for the converter. Procedures describing voltage and mode indicator lamps, lampholder, and fuseholder replacement are provided. Power supply voltages check which is referenced in troubleshooting table 5-3 is provided in paragraph 5-8. Instructions which are common to operation and organizational maintenance are included in chapter 4.

b. Items requiring replacement are listed in TM 11-5895-797-24P.

5-6. Removal

Repairs at organizational category can be made without removing the converter from the rack or removing the top panels.

5-7. Disassembly

WARNING

120 vac is present at the rear panel power connector, front panel POWER switch and fuseholder terminals. Serious injury or DEATH may result from contact with these points.

Replacement of voltage and mode indicator lamps DS2 through DS9 requires unsoldering the attached leads and soldering the leads of the new lamps. The lamps, lampholder, and fuseholders are located on the front panel. To remove these items, open the front panel by loosening six front panel captive mounting screws (fig. 5-1).

Figure 5-1. Inside view of front panel.

a. Replacement of Voltage Indicator Lamps (DS6 through DS9). Replace lamps as follows:

(1) Place POWER switch on front panel to on position.

(2) Open front panel as described in paragraph 5-7.

(3) Check with multimeter that supply voltages and resistances are correct between terminals as indicated in table 5-4. (See fig. 5-1)

(4) Place POWER switch to OFF position.

(5) Check resistances of R4 and R5; disconnect one lead of R4 and R5 before measuring.

(6) Disconnect power cable at power outlet.

(7) Unsolder lamp leads and remove retaining nut to free lamp from front panel (fig. 5-2).

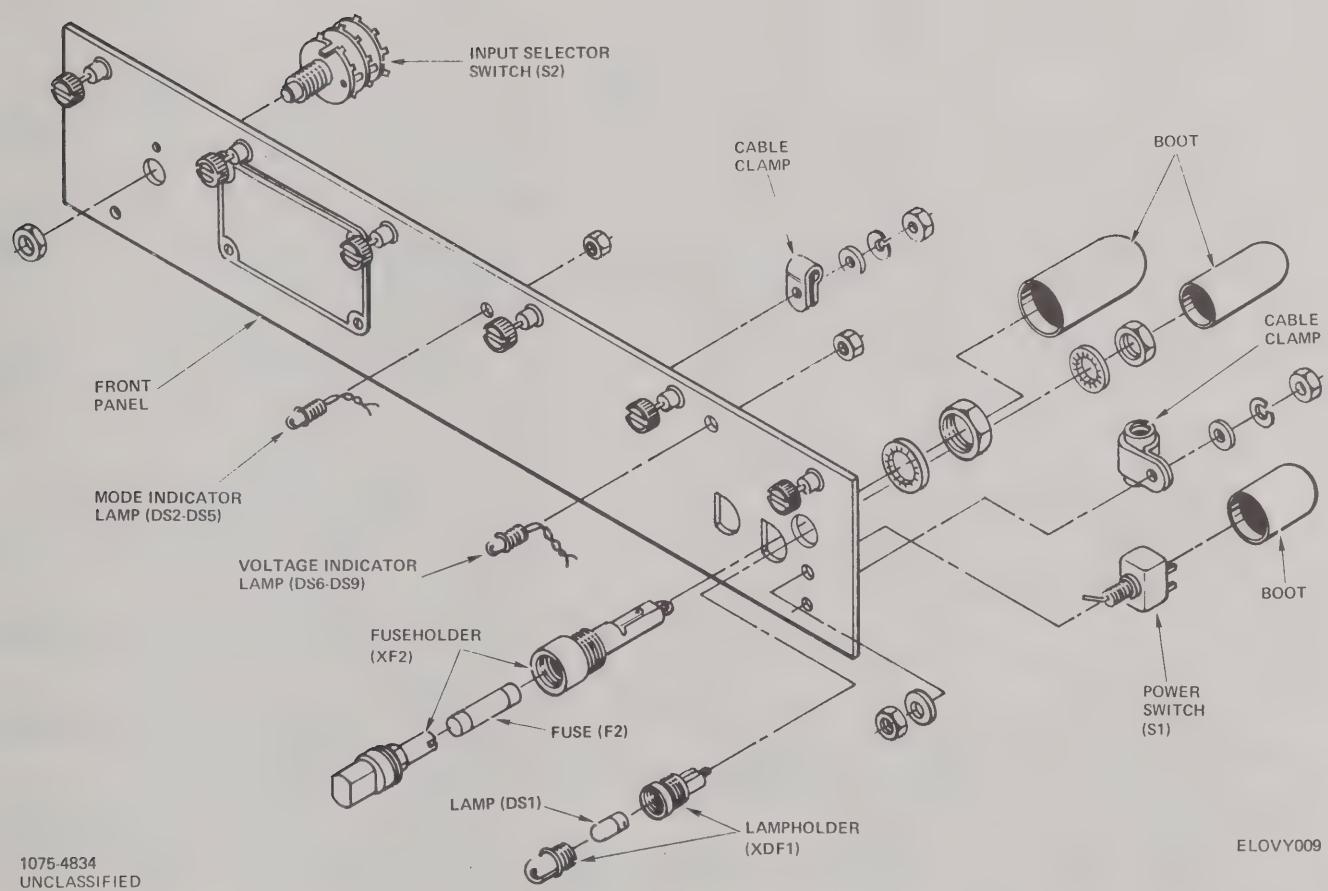


Figure 5-2. Front panel disassembly.

(8) Install new lamp, tighten nut, and solder lamp leads to corresponding terminals.

(9) Close front panel and hold in place with one captive screw.

(10) Connect power cable to power outlet and place POWER switch to on position.

(11) Verify that lamps DS1 and DS6 through DS9 are lighted. Tighten all captive front panel screws.

Table 5-4. Voltage Indicator Lamps and Terminals

Lamp	Terminals	Voltage/ resistance
DS6 (+5 v, transmitter)	E21	+5 v
	E22	Ground
DS7 (+5 v, receiver)	E23	+5 v
	E24	Ground
DS8 (+15 v)	E25	+15 v
	E27	Ground
When DS8 is lighted and R4 is good.	E25 to E26	+5 ±1 v
	E26 to E27	+10 ±1 v
Resistor R4	E26 to E27	160 ±8 ohms
Resistor R4	E26 to E27	160 ±8 ohms
DS9 (−15 v)	E28	−15 v
	E30	Ground
When DS9 is lighted and R5 is good.	E28 to E29	−5 ±1 v
	E29 to E30	−10 ±1 v
Resistor R5	E29 to E30	160 ±8 ohms

b. Replacement of Mode Indicator Lamps (DS2 through DS5). During operation, only one transmitter mode lamp and one receiver mode lamp is lighted at any given time. The lamps should be observed for proper mode indication when the mode of the signals entering the transmitter and receiver is known. Replace lamps as follows:

WARNING

120 vac is present at the rear panel power connector, front panel POWER switch and fuseholder terminals. Serious injury or DEATH may result from contact with these points.

(1) Place POWER switch on front panel to on position.

(2) Open front panel as described in paragraph 5-7.

(3) Check with multimeter that +5 volts is present at terminals E13, E15, E17, and E19.

(4) Check lamps that do not light by jumpering the corresponding terminal to ground (rear of front panel) as listed in table 5-5. (See figure 5-1.)

(5) Replace lamps that do not light as described in paragraph 5-7*a*(4) through (10).

NOTE

Transmitter data presence board 1A4 and receiver digital-to-analog board 1A6 control operation of the mode indicator lamps.

(6) Verify that lamps DS2 or DS3 and DS4 or DS5 are lighted depending upon the mode of the signals entering the transmitter and receiver. If no input signal is applied to the transmitter, the XMTR VOICE (DS2) lamp is lighted. When no input signal is applied to the receiver, the RCVR DATA (DS5) lamp is lighted. Tighten captive front panel screws.

Table 5-5. Test of Mode Indicator Lamps

To check	Jumper to ground terminal
DS2 (XMTR VOICE)	E14
DS3 (XMTR DATA)	E16
DS4 (RCVR VOICE)	E18
DS5 (RCVR DATA)	E20

c. Replacement of Fuseholders XF1 and XF2 and Lampholder XDS1. Replace as follows:

WARNING

120 vac is present at the rear panel power connector, front panel POWER switch and fuseholder terminals. Serious injury or DEATH may result from contact with these points.

(1) Open front panel as described in paragraph 5-7.

(2) Disconnect power cable at power outlet.

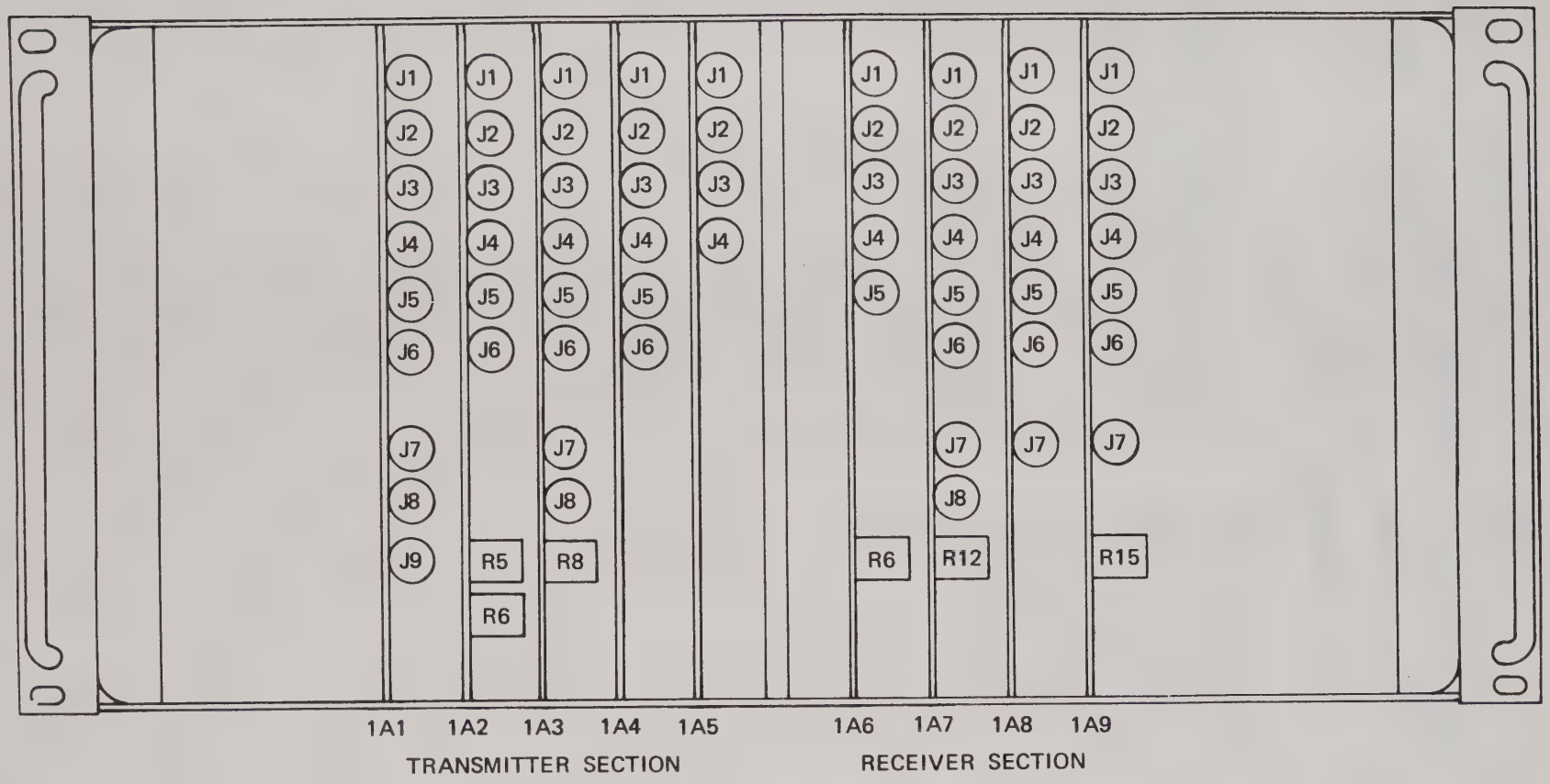
(3) With sharp knife, cut away the insulating plastic boot which covers the item.

(4) Unsolder leads and remove item (fig. 5-2).

(5) Assemble in reverse order of disassembly, install new insulating boot and shrink tight by applying heat.

5-8. Testing During Repair

a. General. Perform preliminary starting procedures given in paragraph 3-3. If required indications are not present, refer to troubleshooting table 7-2. The locations of test jacks and variable resistors are shown in figure 5-3 and become accessible by opening the converter front panel. The common ground connection for the transmitter is test jack 1A1J9, and for the receiver, test jack 1A6J5. These are circuit ground connections, not necessarily chassis ground.



NOTE:

VARIABLE RESISTORS 1A3R8 AND 1A7R12 ARE FOR ADJUSTING TRANSMITTER AND RECEIVER CLOCK FREQUENCIES IF REQUIRED.

VARIABLE RESISTOR 1A9R15 IS FACTORY SET FOR A RECEIVER VOICE OUTPUT LEVEL OF 0 dBm OR +7 dBm DEPENDING UPON STRAPPING OPTION.

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Figure 5-3. Test jacks and variable resistors.

b. Power Supply Voltages Check. Direct current power supply voltages are derived from fixed integrated circuit voltage regulators. If incorrect, refer to table 7-3. With multimeter, measure voltages between the following test jacks:

(1) 1A1J1 (+probe) and 1A1J9 (— probe):

Reading should be +5.0 ± 0.5 vdc for transmitter +5 vdc supply.

(2) 1A1J2 (+ probe) and 1A1J9 (— probe):

Reading should be +15.0 ± 1.5 vdc for transmitter and receiver +15 vdc supply.

(3) 1A1J8 (— probe) and 1A1J9 (+ probe):

Reading should be —15.0 ± 1.5 vdc for transmitter and receiver —15 vdc supply.

(4) 1A6J1 (+ probe) and 1A6J5 (— probe):

Reading should be + 5.0 ± 0.5 vdc for receiver +5 vdc supply.

CHAPTER 6

FUNCTIONING OF EQUIPMENT

Section I. INTRODUCTION

6-1. Purpose of Converter

The converter transmits information in digital form in a communications link from an analgo (voiceband) or digital source. Analog signals are converted to digital signals and digital signals are repeated in the same form.

6-2. General

a. The converter (fig. 6-1) consists of two major independent sections, transmitter and receiver, assembled in a single unit with a common power supply. The transmitter functions as an analog-to-digital converter (voice digitizer) or as a digital repeater. Digital data signals are detected in the data presence circuit, synchronized with the timing generator signals, and applied to the interface amplifier and buffer circuits. Voiceband input signals are amplified, filtered, converted to a digital signal in the analog-to-digital converter, and, through the data presence circuit, applied to the output circuit. The data presence circuit controls the operating mode of the transmitter, voiceband or data.

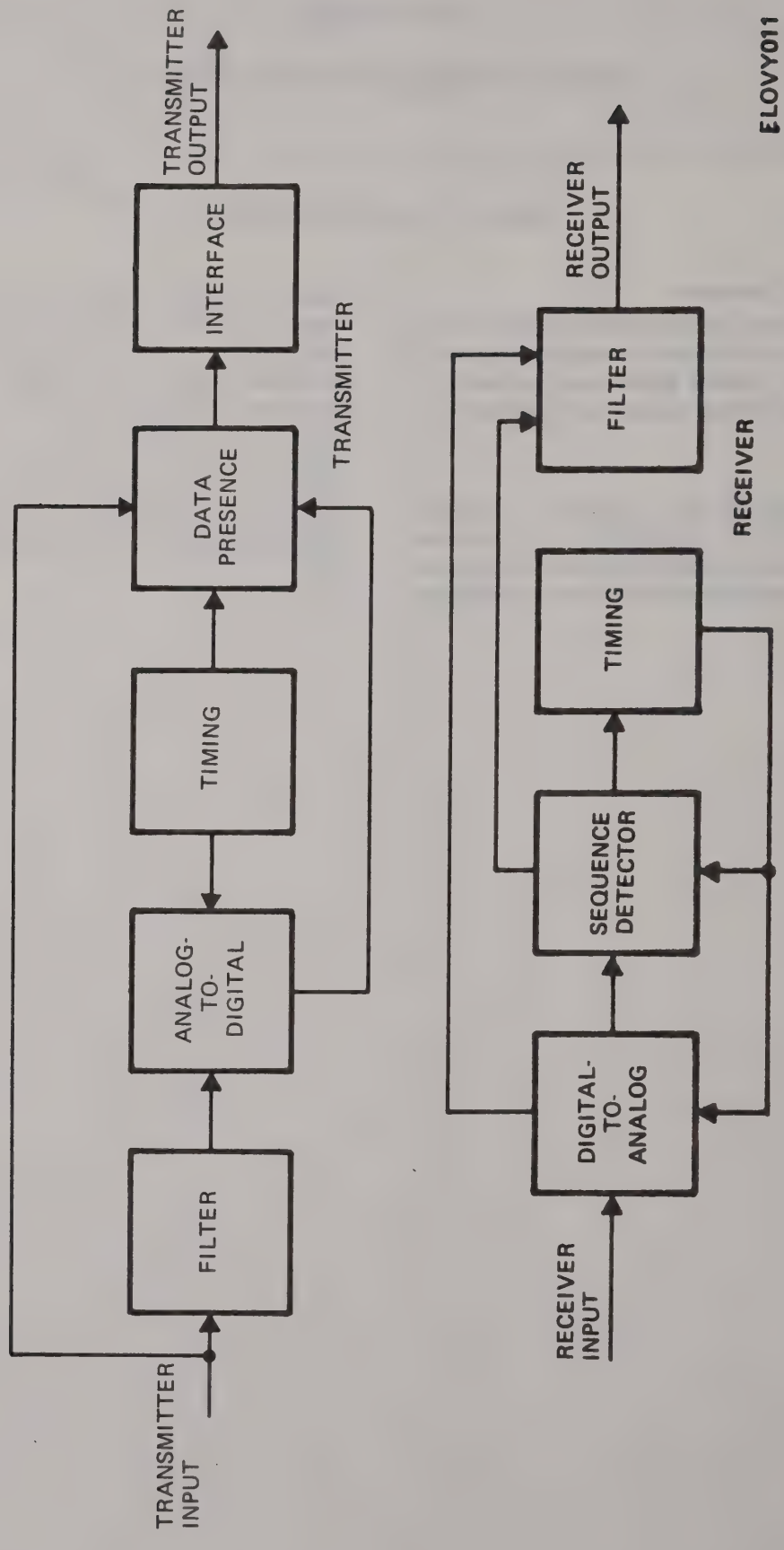


Figure 6-1. Converter block diagram.

b. Receiver operation is similar to the transmitter in reverse order. Input signals are applied to a sequence detector which distinguishes between a digitized voiceband signal and a digital data signal. When a digitized voiceband signal is detected, the receiver operates in the voiceband mode and a digital-to-analog converter approximates the original analog signal. This signal is then filtered and amplified and applied to both the receiver voice output and receiver hybrid output. Digital data signals are reclocked with timing generator signals and, after amplification, applied to the output filter and amplifier circuits.

Section II. GENERAL FUNCTION

6-3. Transmitter Overall Function

(fig. FO-2)

This section describes the overall operation of transmitter filter board 1A1, transmitter analog-to-digital board 1A2, transmitter timing board 1A3, transmitter data presence board 1A4, transmitter interface board 1A5, and input, output and interconnecting circuits.

NOTE

Timing signals of the transmitter are designated sequentially in alphanumeric order; that is B0, C0, C1, C2, D0, D1, D2, D3, F0, G0, etc. The letters B, C, etc. indicate specific steps in the countdown chain; that is, G = 50 kHz, K = 2 kHz, etc. The numbers 0, 1, 2, etc indicate a difference in waveform or duty cycle. A bar over the signal ($\overline{D3}$) indicates the complement of the signal (D3).

a. Inputs, Outputs, and Interconnecting Circuits. The transmitter has three modes of operation and three corresponding input connections, HYBRID, LOW LEVEL voice, and HIGH LEVEL voice.

(1) Voiceband input signals are routed from input connector J1 or J2, through input selector switch S2 to input transformer T3 and to another section of S2. To maintain an impedance match on the 600-ohm input lines resistor R1 is connected across the unused voiceband input. The hybrid input signal from connector J3 is routed through transformer T2 to S2. The selected input signal EW is applied to transmitter filter board 1A1. The hybrid input voiceband or data signal (VORD) is also connected to transmitter data presence board 1A4.

(2) The digital data output of the transmitter is available at DATA connector J5. A synchronizing clock signal is supplied at CLOCK connector J4.

(3) Transmitter connector board 1A10 provides connecting points for interconnections between the printed wiring boards, input and output connectors, and front panel controls and indicators. Chassis connecting points are shown in figure FO-1.

b. Transmitter Filter Board 1A1. Transmitter filter board 1A1 filters and amplifies the applied input signal. Analog voiceband signals are amplified and digital signals are rejected. The gain of the input amplifier is selected by input selector switch S2 to provide approximately the same output level for all three inputs.

(1) The selected input signal EW is applied to the input amplifier. The input amplifier has three fixed gain settings selected by input selector switch S2. The gain is determined by feedback resistor R1, R2, or R19 so that the output level of the transmitter filter is approximately the same for a low level voiceband input, high level voiceband input, or hybrid input.

(2) The amplified output signal of the input amplifier is filtered through a five-pole active elliptic low-pass filter. The analog voiceband signal is passed through the filter but digital signals and other high frequencies are rejected. The analog low-pass filter output capacitively coupled signal LPFOC is applied to transmitter analog-to-digital board 1A2.

c. Transmitter Analog-to-Digital Board 1A2. Transmitter analog-to-digital board 1A2 converts the voiceband signal to an equivalent digital format. The voiceband signal is sampled at an 8-kHz rate and each sample converted to an 8-bit digital signal. Each 8-bit digital signal is reduced to 6 bits resulting in a 48-kbps digitized voice data stream. A 2-kbps pseudorandom sequence is multiplexed into the 48-kbps data stream to yield the 50 kilobit voice data signal (50KBVD).

(1) Input signal LPFOC is sampled at an 8-kHz rate by the sample-and-hold circuit under the control of timing signal $\overline{D3}$. The sampled signal is applied to the comparator and compared with a series of trial voltage levels generated by the digital-to-analog converter. The resultant comparison signal $\overline{COM}$ is stored in the 8-bit storage register at the location selected by timing signals D0, D1, and D2.

(2) Each bit position of the 8-bit storage register is loaded by the $\overline{COM}$ signal in turn, beginning with D0, D1, and D2 equal to 000 (the

most significant bit (MSB) is loaded) and continuing through 111 (the least significant bit (LSB) is loaded). The register is loaded with the digital value of the $\overline{COM}$ signal, converted to an equivalent voiceband signal, then compared with the value of the digitized voice sample signal DVS. If the analog voltage is greater than the DVS signal, nothing more happens until the next bit position of the 8-bit storage register is selected. If, however, the analog voltage is not greater, the output $\overline{COM}$ switches to 1, and a 0 is stored in the LSB position. This sequence continues until all eight bits are established. Eight bits comprise one complete analog-to-digital conversion cycle. Timing signals C1 and C0, synchronized with signals D0 and D3 clear the 8-bit storage register for the next cycle.

(3) The bit pattern from the 8-bit storage register addresses the read only memory (ROM) compressor. The eight bits are compressed into an equivalent six bits and clocked into the parallel-to-serial converter by tyhe 50 kHz clock signal G0. A seventh bit signal SEQ is added by the 7-bit pseudo-random sequence generator. The 7-bit pseudorandom sequence generator, controlled by the 2 kHz clock signals K0 and K1, provides a pseudorandom signal that is multiplexed into the data stream.

(4) The parallel-to-serial converter multiplexes four groups of six data bits, V0 through V5, and the SEQ signal. The loading of the SEQ signal is controlled by signals C2, $\overline{D0}$, and D3. Since data is loaded at a 48-kbps rate (8000 6-bit groups per second), and the parallel-to-serial converter is clocked at a 50-kbps rate, for every 24 data bits loaded in, 25 bits are clocked out. This twenty-fifth bit is the pseudorandom bit inserted into the seventh position of the parallel to serial converter.

(5) The serialized digital data stream output of transmitter analog-to-digital board 1A2 forms the 50KBVD signal and is applied to transmitter data presence board 1A4.

d. Transmitter Timing Board 1A3. Circuits on transmitter timing board 1A3 contain a crystal oscillator and divider circuits to provide the timing signals for the transmitter analog-to-digital and transmitter data presence circuits.

(1) In the voiceband mode the crystal oscillator is free-running and controls the 50 kilobits per second digital output to within three bits per second. In the data repeater mode, the timing circuits are locked to a gated synthetic signal GASYN derived from gating the incoming data stream. Incoming data may vary as much as 20 bits per second without affecting the regeneration.

(2) The crystal-controlled oscillator crystal is series resonant at 7.2 MHz and is temperature compensated. The buffered output of the crystal oscillator can be monitored at test jack J2.

(3) The 7.2-MHz oscillator frequency is divided by 2 and then by 9 to 400 kHz. The divide-by-9 circuit also generates synchronizing signal B0. The 400-kHz signal is further divided in the F/G-scaler and C-scaler. The G-scaler produces 50 kHz clock signals G0 and complement G0. The C-scaler has three different 80-kHz squarewave outputs.

(*a*) CO—On 20 percent, off 20 percent, on 20 percent, off 40 percent.

(*b*) C1—On 40 percent, off 60 percent.

(*c*) C2—On 20 percent, off 80 percent.

(4) The C-scaler 80-kHz output is divided by 2 in the D-scaler to generate clock signal D0 and complement $\overline{D0}$. The 40 kHz signal D0 is then divided by 5 to produce three 8 kHz clock signals with duty cycles as follows:

(*a*) D1—On 20 percent, off 20 percent, on 20 percent, off 40 percent.

(*b*) D2—On 40 percent, off 60 percent.

(*c*) D3—On 20 percent, off 80 percent.

(5) The complement of signal D3, $\overline{D3}$, is also provided. Signal D3 is divided by 2 in the K-scaler resulting in 4 kHz signal K0. Signal K0 is divided by 2 to provide 2 kHz clock signal K1. The synchronizer establishes correct time relationships between the output signals, aligning F0 and G0 output signals with the proper coincidence of the other timing signals.

(6) The frequency controller circuit compares clock signals G0 with the GASYN signal from transmitter data presence board 1A4. The GASYN signal is derived from the incoming digital data. As a result of the comparison, a voltage is applied to the crystal oscillator circuit locking the oscillating frequency to the frequency of the incoming digital signal. The crystal oscillator is free-running when the GASYN signal has a steady true level as a result of a voice input or no input at the HYBRID input connector of the transmitter.

e. Transmitter Data Presence Board 1A4. Transmitter data presence board 1A4 contains circuits that distinguish digital data from voiceband data. The hybrid input signal VORD is subjected to two tests. The signal must have at least a level of minus 15 decibels relative to 1 milliwatt ($\pm$65 millivolts) and a frequency higher than 9500 Hertz. When these two conditions are met, the mode control circuit commands the digital data repeater mode of operation, blocks voiceband signal processing, lights the XMTR DATA lamp on the front panel, reclocks the digital data, and passes the data to the transmitter output.

(1) The input signal VORD is taken directly

from hybrid input transformer T2 and applied to the signal level detector and the hard limiter and zero crossing shaper. The signal level detector compares the peaks of the input signal with an internal reference voltage. When the VORD signal is consistently greater than positive or negative 65 millivolts, the digital signal level signal DSL is true. The low-pass filter prevents an occasional wide swing from reaching the mode control circuit.

(2) The zero crossing detector consists of a hard limiter and signal squaring circuit. The zero crossings of its output coincide with those of the input signal VORD. The one-shot pulse generator develops a 10-microsecond pulse for each positive zero crossing and one for each negative zero crossing. The pulse comparator averages the 10-microsecond pulses and compares the average value with an internal reference. When the average rises above the reference value, digital data frequency signal DDF goes true.

(3) When both DSL and DDF signals are true, the mode control signal MC is true. The MC signal is applied to three circuits. The frequency control circuit is enabled to allow the GASYN signal to control the transmitter oscillator. The lamp driver circuit outputs the XMTR IN DATA signal and lights the XMTR DATA front panel indicator. The data select circuit blocks the 50KBVD signal and enables the DIGITAL DATA signal to be gated from the data synchronizer.

(4) The data synchronizer clocks the digital signal from the hard limiter and zero crossing shaper with the clock signal G0. The selected data signal SEL DATA is shaped, leveled and balanced by the data pulse shaper. The rise and fall slopes of the squarewave are shaped properly and the voltage level is adjusted symmetrically about 0 volt. The data clock shaper circuit performs the identical function for clock signals G0 and $\overline{G0}$.

(5) Digital data output positive (DDOP), digital data output negative (DDON), digital clock output positive (DCOP), and digital clock output negative (DCON) signals are applied to transmitter interface board 1A5.

f. Transmitter Interface Board 1A5. Transmitter interface board 1A5 amplifies and buffers the data and clock output signals from transmitter data presence board 1A4. Transmitter interface board 1A5 contains five independent amplifier-buffer circuits. Data output positive (DOP), data output negative (DON), clock output positive (COP) and clock output negative (CON) are ±3-volt bipolar signals applied to the twin-axial output connectors on the rear panel of the converter to supply a 75-ohm balanced line. The DOPA amplifier supplies a single-ended output as the data output positive amplifier signal (DOPA).

6-4. Receiver Overall Function
(fig. FO-3)

This paragraph describes the overall operation of receiver digital-to-analog board 1A6, receiver timing board 1A7, receiver sequence detector board 1A8, receiver filter board 1A9, and the input, output, and interconnecting circuits.

NOTE

Timing signals of the receiver are designated sequentially in alphanumeric order with an R prefix; for example, RC2, RG0, RK1. The letters C, D, etc. indicate specific steps in the countdown chain; for example, C = 80 kHz, D = 8 kHz. The numbers 0, 1, 2, etc. indicate a difference in the waveform or duty cycle. A bar over a signal ($\overline{RG0}$) indicates the complement of the signal (RG0).

a. Inputs, Outputs, and Interconnecting Circuits. The receiver has three inputs, CLOCK, DATA, and RCVR INPUT (135 Ω) through input connectors J7, J8, and J13, respectively. The two data inputs, DATA and RCVR INPUT (135 Ω), are connected to receiver digital-to-analog board 1A6. The CLOCK input is connected directly to receiver timing board 1A7.

NOTE

The two receiver inputs, DATA and RCVR INPUT (135 Ω), cannot be used simultaneously.

(1) The two outputs of the receiver, HYBRID and VOICE, are coupled to output connectors J9 and J10 through impedance-matching transformers T4 and T5. HYBRID output is designed to drive a 135 ohm balanced line and VOICE output a 600-ohm balanced line.

(2) Connector board 1A11 provides connecting points for interconnections between the printed wiring boards, input and output connectors, and front panel controls and indicators. Chassis connecting points are shown in figure FO-1.

b. Receiver Digital-To-Analog Board 1A6. Receiver digital-to-analog board 1A6 converts the input digital data signal to the equivalent analog voiceband signal when the pseudorandom sequence is detected. The digital data signal is reclocked and retransmitted in digital form when no pseudorandom sequence is detected.

(1) Data is applied to receiver digital-to-analog board 1A6 through connectors J8 and J13. The line termination provides the matching impedance for both the data input positive (DIP) and data input negative (DIN) signals and the data input positive A (DIPA) and data input negative A (DINA) signals.

The positive and negative data is filtered to block high-frequency noise and other spurious signals. The filtered signal, symmetrical about zero, is then shifted to positive pulses on a zero base by the level translator. The output of the level translator, designated incoming data signal ID, is applied to receiver sequence detector board 1A8 and also to data synchronizer 1.

(2) Data synchronizer 1 reclocks the data with receiver 50 kHz clock signal RG0. The synchronized data is applied to the shift register and reclocked in data synchronizer 2 with timing signal $\overline{RG0}$. Reclocked data signal RD is applied to receiver sequence detector board 1A8 and receiver filter board 1A9.

(3) In the shift register, data is clocked in by the RG0 signal. In addition, passed threshold signal PT must be true, indicating that the data is voiceband data and must be converted to an analog signal. The PT signal also energizes lamp driver signal RCVR IN VOICE for a front panel mode indication. The 8 kHz clock signal DD loads six bits of data into the group storage register. Note that in one millisecond, eight groups of six bits (48 bits total) are transferred into the group storage register but that 50 bits are loaded into the shift register. Two bits out of each 50 bits must be omitted from the transfer process. This is inversely analogous to the process of analog-to-digital conversion in the transmitter. In the transmitter, a pseudorandom bit sequence is included to identify an analog voiceband signal. However, in the receiver, the identification bits must be discarded from bit sequence after the identification is made.

(4) The groups of six bits correspond to the groups of six that were compressed from eight in the transmitter. Out of the group of six bits in the group storage register, five are transferred into the read only memory (ROM) expander. The ROM expander is programed to restore the two bits deleted in the transmitter. The sixth bit of the group storage register controls the buffer/inverter. When the sixth bit is true, the buffer/inverter functions as an inverter and when false, functions as a buffer. The sixth bit is inverted and applied to the digital-to-analog converter as the eighth bit. The digital-to-analog converter, identical with that used in the transmitter, develops an output voltage proportional to the value of the eight-bit digital signal. The voltage is maximum positive for bit pattern 11111111 and maximum negative for 00000000 and a midpoint is established at 10000000. The digital-to-analog output signal DAI of the receiver digital-to-analog converter is an unfiltered replica of the analog input to the transmitter. The digital-to-analog conversion process is inhibited by passed threshold signal PT when digital data is detected by the receiver sequence detector circuit.

c. Receiver Timing Board 1A7. Receiver timing board 1A7 generates the timing signals to synchronize operations on receiver digital-to-analog board 1A6 and receiver sequence detector board 1A8. A strapping option allows the timing circuits to be locked to an external 50 kHz clock signal with the 3-volt bipolar format or to the 50 kilobit per-second data input to the receiver. The tracking range of the timing circuits is plus or minus 20 bits per second.

(1) The crystal oscillator is series resonant at 7.2 MHz and is temperature compensated. The buffered RCK output of the crystal oscillator can be monitored at test jack J2. The RCK signal is divided by 2 and then by g to 400 kHz. The 400 kHz is further divided in the CG-scaler generating the 50 kHz clock signals RG0 and $\overline{RG0}$. RG0 and $\overline{RG0}$ are applied to receiver digital-to-analog board 1A6 as the primary data synchronizing signals. The 80 kHz clock signal RC2 is also derived directly from the 400 kHz signal.

(2) Upon receiving RC2, the DK-scaler derives 8 kHz signal DD, 8 kHz signal $\overline{RD2}$, and 2 kHz signals, RK11 and $\overline{RK1}$. The DK-scaler output function is listed below.

(*a*) DD is applied to receiver digital-to-analog board 1A6 to provide the 6-bit loading signal for the group storage register.

(*b*) $\overline{RD2}$ is applied to the receiver digital-to-analog board 1A6 to clear the group storage register.

(*c*) $\overline{RK1}$ is applied to receiver sequence detector board 1A8 to clear input shift register.

(*d*) $\overline{RK1}$ is applied to receiver sequence detector board 1A8 to clear the 4-counter.

(3) The synchronizer circuit aligns 2 kHz clock signals RK1 and $\overline{RK1}$ with the 1200 kHz signal RAI. The resultant synchronizing signal controls the 400 kHz signal.

(4) In addition to being synchronized the 400 kHz signal is also conditioned by the $\overline{HICCUP}$ signal of the hiccup generator. $\overline{HICCUP}$ goes true each time LOAD goes true. The pulse duration is that of a bit length in input data stream RD. The effect is that 2 kHz clock pulse RK1 is delayed one data bit. This is repeated until the pseudorandom sequence in the incoming digitized voiceband signal is recognized by the sequence detector circuitry of receiver sequence detector board 1A8.

d. Receiver Sequence Detector Board 1A8. Receiver sequence detector board 1A8 detects the pseudorandom sequence in the input data signal and controls the operating mode of the receiver. When the pseudorandom sequence is detected, the receiver functions in the voiceband processing mode.

In the absence of the pseudorandom sequence, the receiver functions in the data-repeater mode.

(1) One out of every 25 bits of reclocked data signal RD from receiver digital-to-analog board 1A6, is clocked into the input shift register (4 bits) and into the pseudorandom sequence generator (7 bits) by the RK1 signal. The pseudorandom sequence generator, synchronized by the clocked-in seven bits, starts recirculating by itself and compares its bits in the 4-bit comparator to successive groups of four bits clocked into the input shift register. After comparing each group of four bits, the result is entered into the up/down counter at a rate of 500 per second by the clock signal of the 4-counter. If the up/down counter indicates that 11 or more comparisons were the same, the count comparator applies a true signal to the passed threshold and load flip-flop functions. After 16 comparisons, the 16-counter clocks the results of the count comparator through the passed threshold and load flip-flops. In the voiceband operating mode, PT and $\overline{\text{LOAD}}$ signals are true, indicating to boards 1A6, 1A7 and 1A9 that the signal must be converted back to the original analog signal. When the pseudorandom sequence generator can no longer find its duplicate sequence in the input data signal, the 4-bit comparator loads all zeros into the up/down counter. After a maximum of 5 comparisons, to reduce the counter state from 15 to 10, the passed threshold and load flop-flops are reversed and the receiver reverts to the data mode.

(2) A circuit independent of the sequence detection process, the pulse edge detector, produces a short pulse edge synchronizing signal EDGES for each leading and trailing edge of incoming data signal ID. The EDGES signal is applied to receiver timing board 1A7 to control the crystal oscillator when external synchronization is not employed.

e. Receiver Filter Board 1A9. Receiver filter board 1A9 filters the digital-to-analog converted voiceband signals to duplicate the original signal. This board also contains a switch to pass either the voiceband or data signal and block the other.

(1) The digital-to-analog output signal DAO is filtered by a 5-pole active elliptic low-pass filter which is identical to the one in transmitter filter board 1A1. This filter removes the sampling spectra from the voiceband signal. The filter third stage output is amplified and the receiver voice output signal RVO is applied to the VOICE output connector J10 through the output transformer T5. The digital/voice switch selects either the voiceband signal or the RD signal to the hybrid signal amplifier. The hybrid signal amplifier output, receiver, hybrid output signal RHO, is applied to the HYBRID output connector J9 through output transformer T4.

(2) The passed threshold signals PT and $\overline{\text{PT}}$ control the switching of the digital/switch. The digital data signal is selected and the voiceband signal is blocked when PT is true and vice versa when PT is true.

Section III. DETAIL FUNCTION

NOTE

In discussion of the various detail circuits, if there is no loss of clarity, the component reference designation is usually abbreviated by omission of the next-assembly prefix; this simplifies text and agrees with the practice on the schematic diagram. For example, on transmitter filter board 1A1, the series resistor for input EW is referred to as R3, rather than 1A1R3.

6-5. General

a. The chassis wiring is shown in three illustrations, a chassis schematic diagram (fig. FO-1), a printed board interconnection diagram (fig. FO-4) and an interconnecting wiring diagram (fig. FO-5). The parenthetical designations identifying various leads and starting with the symbol 1A10 or 1A11 indicate the attachment points of those leads on board 1A10 or 1A11 in figure FO-4. Transmitter connector board 1A10 establishes all connections to the five printed circuit boards of the transmitter, and receiver connector board 1A11 services the four boards of the receiver.

b. Input selector switch S2 (fig. FO-1) is a six-pole three-position switch. The switch wipers are designated AW through FW. Wipers AW and BW connect voice input transformer T3 to the high voice input when the switch is in position HIGH LEVEL VOICE, or to the low voice input if the switch is in position LOW LEVEL VOICE or HYBRID INPUT. To maintain an impedance match on the 600-ohm incoming voiceband lines, wipers CW and DW connect a 620-ohm dummy load resistor R1 to the unused voiceband input. Wiper EW of the switch connects the signal lead, identified as EW, to either voice input transformer T3 or hybrid input transformer T2. Wiper FW is used in the selection of a feedback resistor on transmitter filter board 1A1 for gain control.

c. A second input to the transmitter circuits, the

VORD signal, is taken from hybrid input transformer T2 directly. This signal is the means by which an incoming data signal can override selection of the voiceband by input selector switch S2.

6-6. Details of Transmitter

a. Transmitter Filter Board 1A1 (fig. FO-6). The selected signal EW (para 6-5*b*) is applied to input amplifier U1. The gain of U1 is determined by feedback resistor R1, R2, or R19. The appropriate resistor is selected by input selector switch S2 making the output level of the amplifier approximately the same whether the input is low-level voice (—16 dbm, 600 ohms), high-level voice (0 dbm, 600 ohms), or hybrid (0 dbm, 135 ohms).

(1) The output of U1 is filtered by the five-pole active elliptic low-pass filter, consisting of stages U2, U3 and U4 and associated components, and sent out on connector pin 24 as signal LPFOC. This output signal can be monitored at test jack J6. The jumper between connector pins 22 and 38 connects the first and second stages of the filter.

(2) Because the filter is low pass, only voiceband signals are transmitted.

b. Transmitter Analog-to-Digital Board 1A2 (fig. FO-7). The principles of analog-to-digital conversion are described below before the actual description of board 1A2.

(1) The process of analog-to-digital conversion starts by taking an amplitude sample at a given point of the incoming signal and comparing this sample in a comparison circuit with a series of digitally generated trial voltage levels. The first trial voltage if 0 volt which is used to determine the polarity of the sample voltage. The next trial voltage is half the maximum permissible voltage at the proper polarity. In successive steps, each voltage is half that of the preceding step, and is added to the prior accumulation of trial voltages. In any step, if the accumulation of trial voltages does not exceed or is equal to the value of the voltage being converted, a digital 1 is generated and the latest trial voltage remains. If the accumulation exceeds the voltage under test, a digital 0 is generated and the latest trial voltage is rejected. In this way, an accumulation of steps is built up to approximately the value being converted, and a record of the steps remaining in the accumulation is a digital representation of that value. Figure 6-2 gives two simplified examples using four trial voltages. The actual circuit uses eight trial voltages.

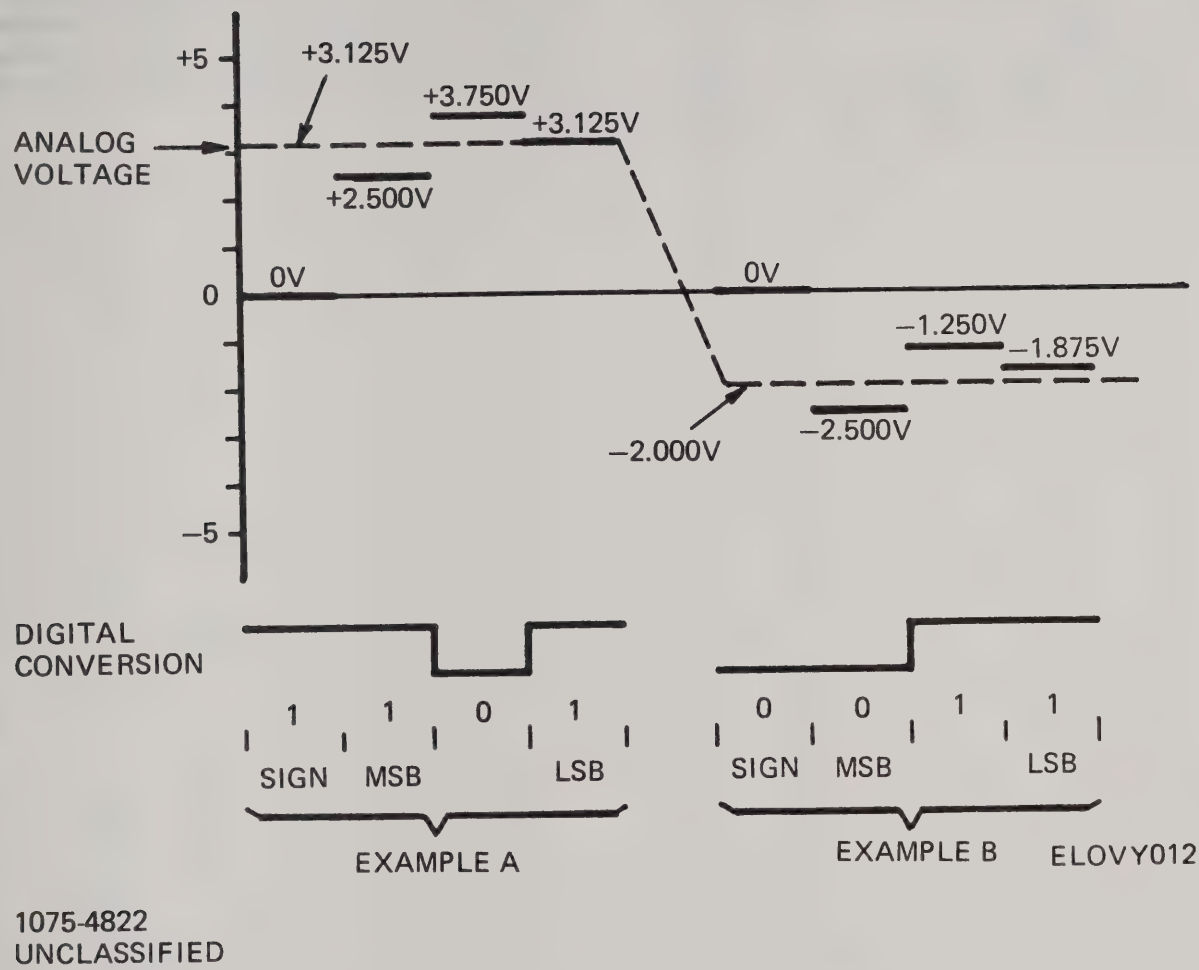


Figure 6-2. Examples of analog-to-digital conversion.

(2) Example A in figure 6-2 shows the conversion of an analog voltage of +3.125 volts to the digital equivalent 1101. The first trial voltage, 0 volt, which when compared with the analog voltage, indicates that the polarity of the analog voltage is positive; therefore a digital 1 is generated for the sign bit. The second trial voltage is +2.500 volts which does not exceed +3.125 volts and therefore a digital 1 is generated for the most significant bit (MSB). The third trial voltage is +1.250 volts which, when added to the remaining +2.500 volts, produces an accumulated trial voltage of +3.750 volts. Because +3.750 volts exceeds +3.125 volts, the +1.250 trial voltage is rejected and a digital 0 is generated for the third digital (second significant) bit. The fourth trial voltage is +0.625 volts which, when added to the remaining +2.500 volts, produces an accumulated trial voltage of +3.125 volts. Because +3.125 volts equals the input analog voltage, a digital 1 is generated for the least significant bit (LSB).

(3) Example B in figure 6-2 shows the conversion of an analog voltage of −2.000 volts to digital equivalent 0011. Again the first trial voltage is 0 volt which when compared with the analog voltage indicates that the polarity of the analog is negative; therefore, a digital 0 is generated for the sign bit. The second trial voltage, −2.500 volts, exceeds −2.000 volts and is therefore rejected. A digital 0 is generated for the MSB. The third trial voltage, −1.250 volts is less than −2.000 volts and therefore remains and a digital 1 is generated. The fourth trial voltage, −0.625 volt when added to the remaining-1.250 volts produces an accumulated 1.875 volts. Because −1.875 volts is less than −2.000 volts, a digital 1 is generated for the LSB. Notice that with a 4-bit analog-to-digital converter, the digital equivalent of the analog voltage is only a

close approximation. In example A of figure 6-2, the fourth trial voltage is precisely equal to the analog voltage. However, in example B and in most instances, the last trial voltage is not precisely equal to the analog voltage.

(4) Conversion is accomplished on the transmitter analog-to-digital board 1A2 (fig. FO-7). Samples of the incoming LOFOC signal are taken at the rate of 8,000 per second by the sample-and-hold circuit consisting of solid state switch U1 and capacitor C1. This is accomplished under control of timing signal D3 (fig. 6-3). The stored voltage on C1 is applied to pin 2 of comparator U6. The other input to U6 is the trial voltage derived from 8-bit storage register U3, digital-to-analog converter U4, and amplifier U5.

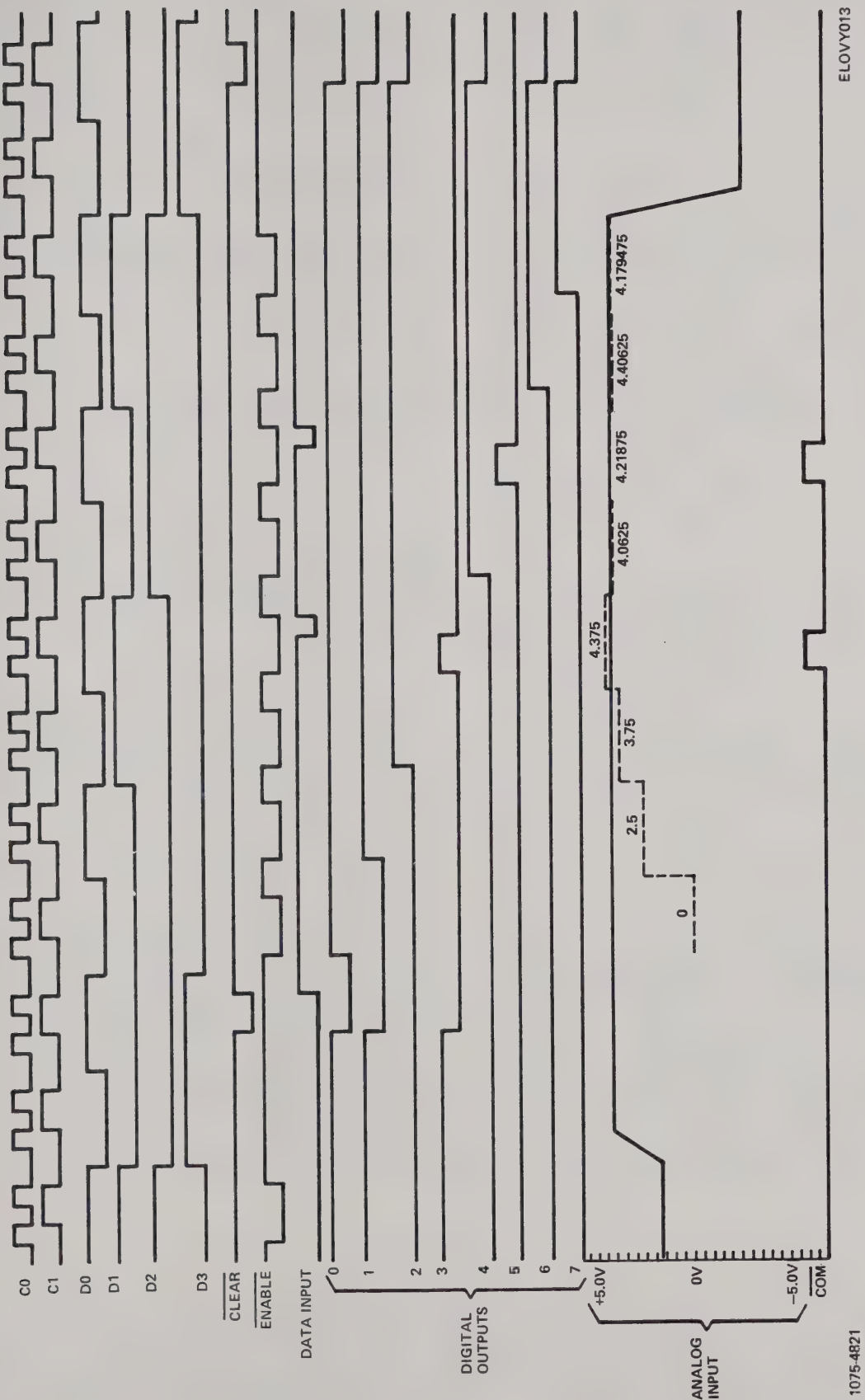


Figure 6-3. Transmitter analog-to-digital board 1A2 waveforms.

(5) The eight outputs of U3 are selected one at a time in sequence by the combinations of timing inputs D0, D1, and D2 connected to pins 1, 2, and 3 respectively. The data input appears at pin 13, a 0 pulse at pin 15 clears the converter, and 0's at both pins 14 and 15 prevent entry of data.

(6) A current is developed at U4, pin 3, as specified by the bit patterns imposed on U4, pins 13 to 6. The total range of this current is determined by the setting of potentiometer R6. The maximum positive current occurs for a bit pattern 11111111, the midpoint for 10000000, and the maximum negative for 00000000. The full scale range is set to 2 milliamperes. The actual value of the midpoint of this range is set by potentiometer R5 which controls a bias voltage from Zener diode CR1. The midpoint of the range is set to 0 milliamperes, so that the output varies between −1 and +1 milliampere.

(7) Amplifier U5 converts the current form U4, pin 3, to a voltage which appears at U5, pin 6. This voltage, which is determined by the bit pattern, is compared by U6 with the sample of the incoming analog signal.

(8) The control on inputs to storage register U3 rests in three interrelated circuits; the timing inputs at U3, pin 15, the input data at pin 13, and the $\overline{\text{COM}}$ signal from U6, pin 7. When the three inputs D0, D3, and C1 from the timing circuits simultaneously have a value 1, a 0 pulse is applied from NAND gate U2, pin 6, to clear U3. Input data at U3, pin 13, is supplied by the latch circuit with outputs at U14, pins 6 and 8. The latch circuit delivers a 1 as data following detection of coincidence of 0's timing inputs C1 and C0 by exclusive OR gate U9, pin 3 and pin 6, and NOR gate U14, pin 3. The latch circuit delivers a 0 data following detection by NOR gate U2, pin 12, of a coincidence of three 1's, two from timing inputs C1 and C0, and the third, the comparison signal $\overline{\text{COM}}$, from comparator U6, pin 7.

(9) The loading of data at U3, pin 13, takes place as follows: Assume U3 to be cleared, the output at U14, pin 6, to be 1, and the bit position at U3, pin 4, selected by the inputs at pins 1,2, and 3. The 1 from the latch appears at U3, pin 4. This is converted to an analog voltage by analog-to-digital converter U4, amplified by U5, and input to the comparator at U6, pin 3. If the analog voltage is greater than that of the sample, nothing more happens until the next bit position at U3, pin 5, is selected. If the analog voltage is not greater, the output $\overline{\text{COM}}$ signal from U6 becomes 1, causing the latch circuit to change the bit being stored at U3, pin 4, from a 1 to a 0. This sequence continues until the value of all eight bits are established. When this happens one complete analog-to-digital conversion has taken place. The bit pattern from U3 serves to address the read only memory (ROM) U7, which compresses the 8-bit data into six bits (table 6-1), and delivers these six bits in groups of four to the 7-bit shift register U8; the seventh bit is provided by a pseudorandom sequence generator. Reading out of U8 is under control of 50 kHz clock signal GO. The output of U8 is reclocked by flip-flop U10, pin 5.

(10) Since readout is done at the rate of 50 kbps, and loading of data at the rate of 48 kbps (that is at the rate of 8000 6-bit groups per second), for every 24 data bits loaded, 25 are read out. This twenty-fifth bit is the pseudorandom bit inserted at the seventh position of the shift register acting as a parallel-to-serial converter.

(11) The final output of this board is labeled 50KBVD and goes to transmitter data presence 1A4.

(12) The pseudorandom sequence generator is comprised of a series of seven flip-flops. The final output is at pin 15 of flip-flop U12; D and CL mark the data input and the clocking inputs respectively. The seven flip-flop outputs going to inputs 1, 2, 3, 4, 5, 6, and 11 of NAND gate U13 are the complements of the outputs of the individual flip-flops, so that if all 0's are in the flip-flops which can only occur at initial power turn-on, the output at U13, pin 8, will cause a 1 to be inserted in the group, when the timing signal K0 at U13, pin 12, permits. Outputs from the third (U11, pin 9) and last (U12, pin 15) flip-flops are inputs to the exclusive OR gate U9 at pins 9 and 10. The output at U9, pin 8, is the input to pin 12 of the first flip-flop U10 of the pseudorandom sequence generator.

Table 6-1. 1A2U7 Bit Outputs as a Function of Inputs

INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT
AAAAAAAA 76543210	DDDDDD 654 321	AAAAAAAA 76543210	DDDDDD 6543 21	AAAAAAAA 76543210	DDDDDD 6543 21	AAAAAAAA 76543210	DDDDDD 6543 21
00000000	000000	00100000	000011	01000000	001000	01100000	001111
00000001	000000	00100001	000011	01000001	001000	01100001	001111
00000010	000000	00100010	000100	01000010	001000	01100010	001111
00000011	000000	00100011	000100	01000011	001000	01100011	010000
00000100	000000	00100100	000100	01000100	001001	01100100	010000
00000101	000000	00100101	000100	01000101	001001	01100101	010000
00000110	000001	00100110	000100	01000110	001001	01100110	010000
00000111	000001	00100111	000100	01000111	001001	01100111	010001
00001000	000001	00101000	000100	01001000	001001	01101000	010001
00001001	000001	00101001	000100	01001001	001010	01101001	010001
00001010	000001	00101010	000101	01001010	001010	01101010	010010
00001011	000001	00001011	000101	01001011	001010	01101011	010010
00001100	000001	00101100	000101	01001100	001010	01101100	010010
00001101	000001	00101101	000101	01001101	001010	01101101	010011
00001110	000001	00101110	000101	01001110	001011	01101110	010011
00001111	000001	00101111	000101	01001111	001011	01101111	010011
00010000	000010	00110000	000101	01010000	001011	01110000	010100
00010001	000010	00110001	000110	01010001	001011	01110001	010100
00010010	000010	00110010	000110	01010010	001011	01110010	010101
00010011	000010	00110011	000110	01010011	001100	01110011	010101
00010100	000010	00110100	000110	01010100	001100	01110100	010110
00010101	000010	00110101	000110	01010101	001100	01110101	010110
00010110	000010	00110110	000110	01010110	001100	01110110	010111
00010111	000010	00110111	000110	01010111	001101	01110111	010111
00011000	000010	00111000	000111	01011000	001101	01111000	011000
00011001	000011	00111001	000111	01011001	001101	01111001	011001
00011010	000011	00111010	000111	01011010	001101	01111010	011010
00011011	000011	00111011	000111	01011011	001110	01111011	011011
00011100	000011	00111100	000111	01011100	001110	01111100	011100
00011101	000011	00111101	000111	01011101	001110	01111101	011101
00011110	000011	00111110	001000	01011110	001110	01111110	011110
00001111	000011	00111111	001000	01011111	001111	01111111	011111
10000000	100000	10100000	110000	11000000	110111	11100000	111100
10000001	100001	10100001	110001	11000001	110111	11100001	111100
10000010	100010	10100010	110001	11000010	111000	11100010	111100
10000011	100011	10100011	110001	11000011	111000	11100011	111100
10000100	100100	10100100	110001	11000100	111000	11100100	111100
10000101	100101	10100101	110010	11000101	111000	11100101	111100
10000110	100110	10100110	110010	11000110	111000	11100110	111100
10000111	100111	10100111	110010	11000111	111000	11100111	111101
10001000	101000	10101000	110010	11001000	111001	11101000	111101
10001001	101000	10101001	110011	11001001	111001	11101001	111101

Table 6-1. 1A2U7 Bit Outputs as a Function of Inputs—Continued

INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT
AAAAAAAA 7 6 5 4 3 2 1 0	DDDDDD 6 5 4 3 2 1	AAAAAAAA 7 6 5 4 3 2 1 0	DDDDDD 6 5 4 3 2 1	AAAAAAAA 7 6 5 4 3 2 1 0	DDDDDD 6 5 4 3 2 1	AAAAAAAA 7 6 5 4 3 2 1 0	DDDDDD 6 5 4 3 2 1
10001010	101001	10101010	110011	11001010	111001	11101010	111101
10001011	101001	10101011	110011	11001011	111001	11101011	111101
10001100	101010	10101100	110011	11001100	111001	11101100	111101
10001101	101010	10101101	110100	11001101	111001	11101101	111101
10001110	101011	10101110	110100	11001110	111001	11101110	111101
10001111	101011	10101111	110100	11001111	111010	11101111	111101
10010000	101100	10110000	110100	11010000	111010	11110000	111110
10010001	101100	10110001	110100	11010001	111010	11110001	111110
10010010	101100	10110010	110101	11010010	111010	11110010	111110
10010011	101101	10110011	110101	11010011	111010	11110011	111110
10010101	101101	10110100	110101	11010100	111010	11110100	111110
10010101	101101	10110101	110101	11010101	111010	11110101	111110
10010110	101110	10110110	110101	11010110	111011	11110110	111110
10010111	101110	10110111	110110	11010111	111011	11110111	111110
10011000	101110	10111000	110110	11011000	111011	11111000	111110
10011001	101111	10111001	110110	11011001	111011	11111001	111110
10011010	101111	10111010	110110	11011010	111011	11111010	111111
10011011	101111	10111011	110110	11011011	111011	11111011	111111
10011100	101111	10111100	110111	11011100	111011	11111100	111111
10011101	110000	10111101	110111	11011101	111011	11111101	111111
10011110	110000	10111110	110111	11011110	111100	11111110	111111
10011111	110000	10111111	110111	11011111	111100	11111111	111111

c. Transmitter Timing Board 1A3 (fig. FO-8). The operation of the transmitter depends upon the pulse frequency, duration, and time relationships of the numerous timing signals. These signals are generated on transmitter timing board 1A3. See figure 6-4 for the timing diagram of the signals on board 1A3.

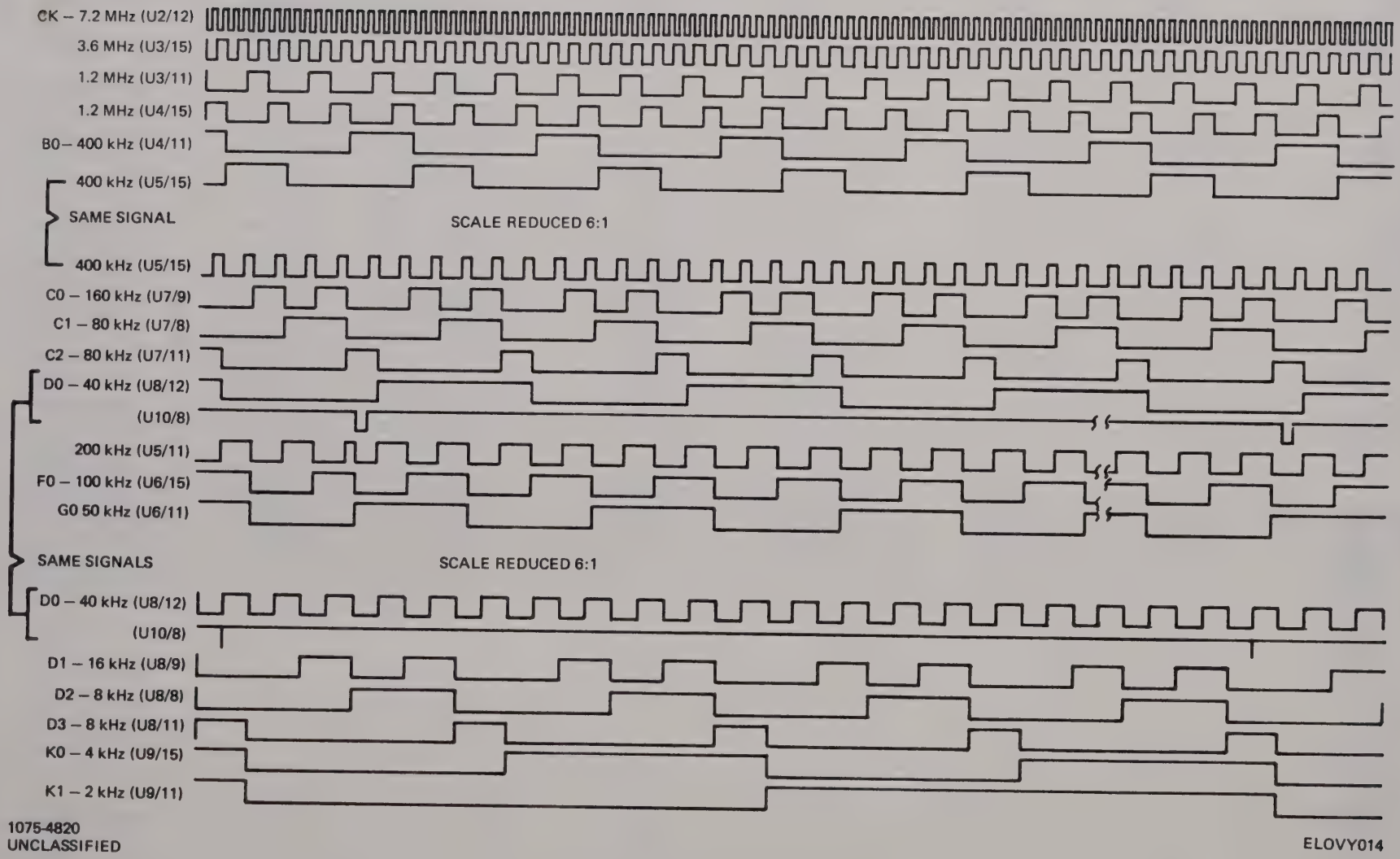


Figure 6-4. Transmitter timing board 1A3 waveforms.

(1) All timing signals are derived from the output of a crystal-controlled oscillator. The basic oscillator circuit consists of R10, U2, C2, R11, L1, C3, CR4, and Y1. Crystal Y1 is the frequency controlling crystal, cut to be series resonant at 7.2 MHz. Variation of voltage across voltage-variable capacitor CR4 varies the frequency over a small range. Variable resistor R8 is used to vary the voltage across CR4 for fine adjustment of the oscillator frequency and CR2 and CR3 are thermally variable elements used for temperature compensation of the oscillator. The circuit through R5 is explained in (7) below.

(2) The buffered output of the oscillator appears at U2, pin 12. From this point, the signal goes through a series of frequency dividers and pulse controls to give the desired outputs.

(3) From the left-to-right at the top of figure FO-8 are one divide-by-2 and two divide-by 3 sections so that the output from U5, pin 15 is 7.2 MHz divided by 18, or 400 kHz. This 400-kHz signal is split into two branches. The branch to U5, pin 6 goes to three divide-by-2 sections producing the 100 kHz output FO from flip-flop U6, pin 15 and is brought out to connector pin 6. The 100 kHz is further divided to yield 50 kHz clock signal GO and complement $\overline{GO}$, produced at flip-flop U6, pins 11 and 10. These signals are brought out to connector pins 8 and 7, respectively.

(4) The second branch of the 400 kHz signal goes to another division system. Decade scalers U7 and U8, each has a divide-by-2 section with input at pin 14 and output at pin 13 (unused in U7), and a divide-by-5 section with input at pin 1 and output at pins 8, 9, and 11. The three outputs of the divide-by-5 section differ in wave form. From pin 8, the square wave is on 40 percent, off 60 percent. From pin 9, a pair of pulses is issued, on 20 percent, off 20 percent, on 20 percent, off 40 percent. This is the reason frequency measurement by pulse counting will show double the rate of pattern repetition. From pin 11, the square wave is on 20 percent, off 80 percent.

(5) The 400 kHz wave enters the divide-by-5 section of U7 at pin 1, and the three 80 kHz outputs are as follows:

(*a*) From pin 8, as signal C1, to connector pin 24.

(*b*) From pin 9, as signal C0, to connector pin 26.

(*c*) From pin 11, as signal C2, to connector pin 12, and also to the divide-by-2 sections of decade scaler U8.

(6) The resulting 40 kHz output signal D0, from U8, pin 12, is brought to connector pin 20; also, after inversion, as signal $\overline{DO}$ to connector pin 23. DO is also the input to the divide-by-5 section of U8, which produces 8 kHz outputs as follows:

(*a*) From pin 8, as signal D2, to connector pin 15.

(*b*) From pin 9, as signal D1, to connector pin 16.

(*c*) From pin 11, as signal D3, to connector pin 18 and after inversion, as signal $\overline{D3}$, to connector pin 22. Signal $\overline{D3}$ also goes to flip-flop U9, pin 1, where the frequency is divided by 2. The 4 kHz signal out of this flip-flop goes to connector pin 19 and to U9, pin 6. In second flip-flop U9 the frequency is again divided by 2, and 2 kHz signal K1 is brought to connector pin 14.

(7) Two other circuits are on this board. NAND gate U10 establishes correct time relationships between the outputs, aligning outputs FO and GO with the proper coincidence of the other timing signals. The other subsidiary circuit with exclusive OR gate U1 compares 50 kHz clock signal GO with the gated synthetic signal GASYN from transmitter data presence board 1A4. GASYN is a pulse signal derived from incoming digital data. As a result of the comparison, a voltage is applied to CR4 through R5 which locks the oscillator frequency to the frequency of the incoming signal. If GASYN has a steady logic 1 value, as a consequence of voiceband input or no input at all at the hybrid terminal of the equipment, then the clock is free-running.

d. Transmitter Data Presence Board 1A4 (fig. FO-9). The circuits in this printed wiring board are designed to enable digital data at the hybrid input to the transmitter to override any selection of voiceband input made by the front panel selector switch. Two tests are applied to indicate the presence of digital data. The incoming signal must have a voltage swing wider than ±65 millivolts, equivalent to a level of −15 dbm at 135 ohms, and the signal must cross the zero baseline at a rate greater than 9,500 times per second.

(1) The input signal VORD is taken directly from hybrid input transformer T2 (fig. FO-1). The signal is fed to comparators U2 and U3 and compared with a positive and negative 65-millivolt reference voltage derived from the +15 and −15-volt sources by voltage dividers. Whenever the input signal goes beyond limits, ±65 millivolts, a 0 signal appears at pin 7 of U2 or U3, depending on the direction of swing. Low-pass filter R40-C9 prevents the transmission of the 1 output during data bit transitions. The input must consistently swing beyond the threshold of ±65 millivolts to develop the 0 output. Inverter U8 has 1 signal at pin 12 for digital data input and a 0 signal for voiceband input.

(2) The second test for the presence of data, the

rate at which the signal crosses the zero line, is made by the circuit starting with U1, which is a comparator and hard limiter. The output at U1, pin 7 is a square wave with zero crossings which coincide with those of the incoming signal VORD. If VORD is a digital signal, U1 also restores any loss of squareness.

(3) The output of U1 goes to U5, a pair of one-shot pulse generators. A negative-going edge on the pulse from U1 develops a 10-microsecond pulse to a logic 0 at U5, pin 7. Similarly, a positive-going edge on the pulse from U1 develops the 10-microsecond zero pulse at U5, pin 9. Both of these pulses are fed into NOR gate U6, pins 1 and 2, to produce an output of positive pulses at pin 3 corresponding to the combination of rise and fall through zero of the incoming signal. (That is, a 1 bit between two 0 bits of data will produce two short pulses at U6, pin 3). The filter string, R23-C16-R24, averages the pulses so that the voltage at comparator U7, pin 2, rises with increasing frequency of transitions.

(4) When the voltage at comparator U7, pin 2, rises above a threshold valued determined by voltage divider R25-R26 the signal at U7, pin 7, becomes 1. The values of circuit elements are selected so that the 1 signal appears at U7, pin 7, when the pulses out of U5 are produced at a rate of over 9500 per second to indicate that the data input is a digital, and not a voiceband signal.

(5) The results of both tests of the signal VORD (the outputs from comparator U7, pin 12) control NAND gate U9, with output at U9, pin 8, being a 0 for data, and 1 for voiceband. When it is 1, it enables a pair of inverters in paralled (U10, pins 1,2, 13 and 12) which light the panel indicator XMTR VOICE by grounding the XMTR VOICE output at connector pin 30. Resistors R28 and (for XMTR DATA) R29 maintain a continous current through the indicator lamps, sufficient to keep the filament warm but not visible, thereby reducing turn-on transients. The output from NAND gate U9, pin 8, also goes to NAND gate U6, pin 9; when VORD is digital, the 0 at pin 9 prevents the 50 KBVD signal, or the bits representing the voice conversions, from further passage. Also, when VORD is digital, the output from U9, pin 8, is inverted to a 1 at inverter U9, pin 10. This signal causes the XMTR DATA indicator to light and permits passage of the digital signals entering NAND gate U6, pin 13. The output at NOR gate U9, pin 12, is the inversion of whichever input (U9, pin 13 or 1) is effective. It appears after reinversion to the normal polarity as the digital data output positive signal DDOP; and after two inversions to the negative polarity, as the digital data output negative signal DDON. The networks immediately preceding the DDOP and DDON outputs (connector pins 38 and 36) are for shaping and leveling the output wave; that is, determining the rise and fall slopes of the square wave, and adjusting the voltage level so that they are symmetrical about 0 volt.

(6) In addition to the branch of the input signal that goes to the one-shots U5, there is also an input to flip-flop U4, pin 12. This flip-flop is clock-controlled by input GO at pin 11 to provide accurate timing. The output of U4, pin 9, is the data signal previously referred to as the input to NAND gate U6, pin 13.

(7) The other data-related output from transmitter data presence board 1A4 is identified as the gated synthetic signal GASYN. When input signal VORD is digital, the same signal that controls the XMTR DATA indicator current also turns on NAND gate U6 at pin 5. This action permits the pulse stream from NOR gate U6, pin 3, to pass and become the signal GASYN, and when the input signal VORD is voiceband, or is absent, GASYN has the value 1.

(8) On the same board for convenience, but independent of the data presence circuits, are a pair of networks similar to those ahead of connector pins 38 and 36, but affecting 50 kHz clock signals GO and $\overline{GO}$ to give clock signals of appropriate shape and level at pin 34 (DCOP signal) and pin 35 (DCON signal).

e. Transmitter Interface Board 1A5 (fig. FO-10). This board consists of four conventional and independent amplifier-buffer circuits and an additional circuit serviced by amplifier U1. The input signals DDOP, DDON, DCOP and DCON are received from the transmitter data presence board 1A4 and the output signals, data output positive (DOP), data output negative (DON), clock output positive (COP), and clock output negative (COP), go to the twin axial output connectors on the rear panel of the equipment, to supply 75-ohm loads. The DDON input signal is also amplified in U1 and provides the DOPA signal used to drive the 135-ohm output transformer which produces the XMTR OUTPUT (135 Ω) signal at rear panel connector J12. The gain of the amplifier circuit produces a 0 db ±1 db (135 Ω) signal across J12 and J12 is teminated in 135 ohms.

6-7. Details of Receiver

a. Receiver Digital-to-Analog Board 1A6 (fig. FO-11). There are two possible ways in which 50 kbps digital data can be applied to the receiver.

(1) One way is for the incoming DATA IN signal from the input connector J8 (fig. FO-1) on the rear panel of the equipment to enter receiver digital-to-analog board 1A6 as data in positive (DIP) and data in negative (DIN) signals on connector pins 6 and 8.

Resistor R1 provides the proper 75-ohm termination. the other way is for the transformer-coupled RCVR INPUT (135 Ω) signal, applied to rear panel connector J13, to appear as DIPA and DINA signals at connector pins 38 and 35 of board 1A6. In this case, R18 and R21 provide appropriate termination. The DIP and DIN signals are fed into comparator U1 through R3 and R2 and the DIPA and DINA signals through R19 and R17. The signals are low-pass filtered by C1 and C2 to prevent high frequency noise and other spurious signals from getting through and giving false indications. Comparator U1 produces a TTL compatible output. Note that only one of the inputs, either DATA/RCVR INPUT or RCVR INPUT (135 Ω), should be used at any one time. Simultaneous use would not allow the output of U1 to accurately reflect the bit stream of either input.

(2) The incoming data signal ID from U1, pin 7, is distributed three ways. It goes directly to the pulsed edge detector on receiver sequence detector board 1A8 which outputs the edge synchronization signal EDGES. The EDGES signal is transmitted to receiver timing board 1A7, and depending on the strapping of terminals E1, E2 and E3, may be used to control the oscillator frequency. If the EDGES signal is used, terminals E2 and E3 are strapped; strapping E1 and E2 is done when an external clock is used for control. The ID signal also enters flip-flop U11, pin 2, on receiver digital-to-analog board 1A6 and is reclocked by 50 kHz signal RG0 and at U11, pin 5, becomes the pulse input for the digital-to-analog conversion process, and also the input for flip-flop U11, pin 12. At this point the signal is again reclocked by RG0; the final output from pin 9 going through connector pin 12 as the reclocked data signal RD. After passing through buffer and filter stages and the output transformer T4 (fig. FO-1), the ID signal eventually becomes the hybrid output at J9 on the rear panel if it represents digital data and not an analog conversion.

(3) The signal from flip-flop U11, pin 5 ((2) above), becomes the input to the digital-to-analog conversion process by entering shift register U2 at pin 3. In U2, the successive bits are assembled in groups of six, the assembly process being clocked by the RGO signal at U2, pin 9. The groups are dumped in parallel (with the bit at U2, pin 2, inverted by U9, pin 6) at the rate of 8 kHz into register U3, as controlled by the 8 kiloHertz clock signal DD at U3, pin 9. Note that in 1 millisecond, eight groups of six bits (48 bits total) are transferred into U3, but that 50 bits are fed into U2; consequently, two out of every 50 bits must be omitted from the transfer process. This is inversely analogous to the process of analog-to-digital conversion in the transmitter, which permits inclusion of a bit sequence to identify a voiceband signal. In the receiver, however, the identification bits must be discarded from the bit sequence, representing the original analog signal, after they have served their purpose. The problem still remains which bit in a sequence of 25 bits is the one to be dropped; this is essentially the same problem as the determination of which bits are to be recognized as distinguishing voiceband data from digital data.

(4) Assume that the identifying bits are omitted, the groups of six bits then correspond to the groups of six bits (compressed from eight) that were transferred out of compressor U7 on transmitter analog-to-digital board 1A2. Out of the group of six bits, five are transferred through exclusive OR gates into expander U6, which is designed to restore the effect of the two bits deleted at the transmitter. From U6 the seven output bits are transferred into digital-to-analog converter U8 through another battery of exclusive OR gates. The sixth bit out of U3, pin 2, controls the exclusive OR gates, so that if the bit has the value 1, the exclusive OR gates act as inverters, and if 0, the exclusive OR gates are merely buffers. This sixth bit also becomes the eighth bit, after inversion, for entry into U8. Inverter U8 is identical with digital-to-analog converter U4 on transmitter analog-to-digital board 1A2, and develops an output current depending upon the incoming bit pattern, a maximum positive for 11111111, a midpoint for 10000000 and a maximum negative for 00000000. The current is then converted to a voltage at U10, pin 6. This voltage is an unfiltered replica of the analog input to the transmitter, and it appears at output pin 14 as digital-to-analog output signal DAO. If the transmitted signal is digital data, not analog, a passed threshold signal PT from receiver sequence detector board 1A8 becomes 0 instead of 1, and shift register U2 is disabled through pin 1.

(5) On this board are the inverters controlling the front panel receiver mode indicating lights. When PT is 1, the two inverters (U9, pins 11, 10, and 13, 12) ground connector pin 20, and cause the RCVR VOICE lamp to light; similarly, when $\overline{PT}$ is 1, the RCVR DATA lamp is lighted. Resistors R15 and R16 keep the filaments of the indicator lamps warm but not visible, to reduce starting surges.

(6) The reconstruction of bits 6 and 7 is accomplished by expander U6, a read only memory signal ROM, specially programmed to perform a function inverse to the one performed in the transmitter. Expander U6 operates in conjunction with the inverter U9, pins 9, 8, and the two groups of exclusive OR gates.

(7) Table 6-2 contains a list of the seven-bit outputs of U6 as a function of the five-bit inputs.

b. Receiver Timing Board 1A7 (fig. FO-12, 6-5 and 6-6). The timing circuits for the receiver are similar to those of the transmitter (para. 6-5*c*). A crystal controlled oscillator operating at 7.2 MHz is followed by cascaded frequency dividers which produce the timing signals needed for the receiver circuits. Relationships between the receiver timing signals are shown in figure 6-5.

Table 6-2. 1A6U6 Bit Outputs as a Function of Inputs

U6 Inputs					U6 Outputs						
Pin No. 14	13	12	11	10	7	6	5	4	3	2	1
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	0	0	0	1	1
0	0	1	0	0	0	0	0	0	1	0	0
0	0	1	0	1	0	0	0	0	1	0	1
0	0	1	1	0	0	0	0	0	1	1	0
0	0	1	1	1	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	1	0	0	1
0	1	0	0	1	0	0	0	1	0	1	1
0	1	0	1	0	0	0	0	1	1	0	1
0	1	0	1	1	0	0	0	1	1	1	1

Table 6-2. 1A6U6 Bit Outputs as a Function of Inputs —Continued

U6 Inputs					U6 Outputs						
Pin No. 14	13	12	11	10	7	6	5	4	3	2	1
0	1	1	0	0	0	0	1	0	0	0	1
0	1	1	0	1	0	0	1	0	1	0	1
0	1	1	1	0	0	0	1	0	1	1	1
0	1	1	1	1	0	0	1	1	0	1	1
1	0	0	0	0	0	0	1	1	1	1	1
1	0	0	0	1	0	1	0	0	0	1	1
1	0	0	1	0	0	1	0	0	1	1	1
1	0	0	1	1	0	1	0	1	0	1	1
1	0	1	0	0	0	1	0	1	1	1	1
1	0	1	0	1	0	1	1	0	1	0	0
1	0	1	1	0	0	1	1	1	0	0	1
1	0	1	1	1	0	1	1	1	1	1	1
1	1	0	0	0	1	0	0	0	1	0	1
1	1	0	0	1	1	0	0	1	0	1	1
1	1	0	1	0	1	0	1	0	0	1	0
1	1	0	1	1	1	0	1	1	0	1	0
1	1	1	0	0	1	1	0	0	0	1	0
1	1	1	0	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	0	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1

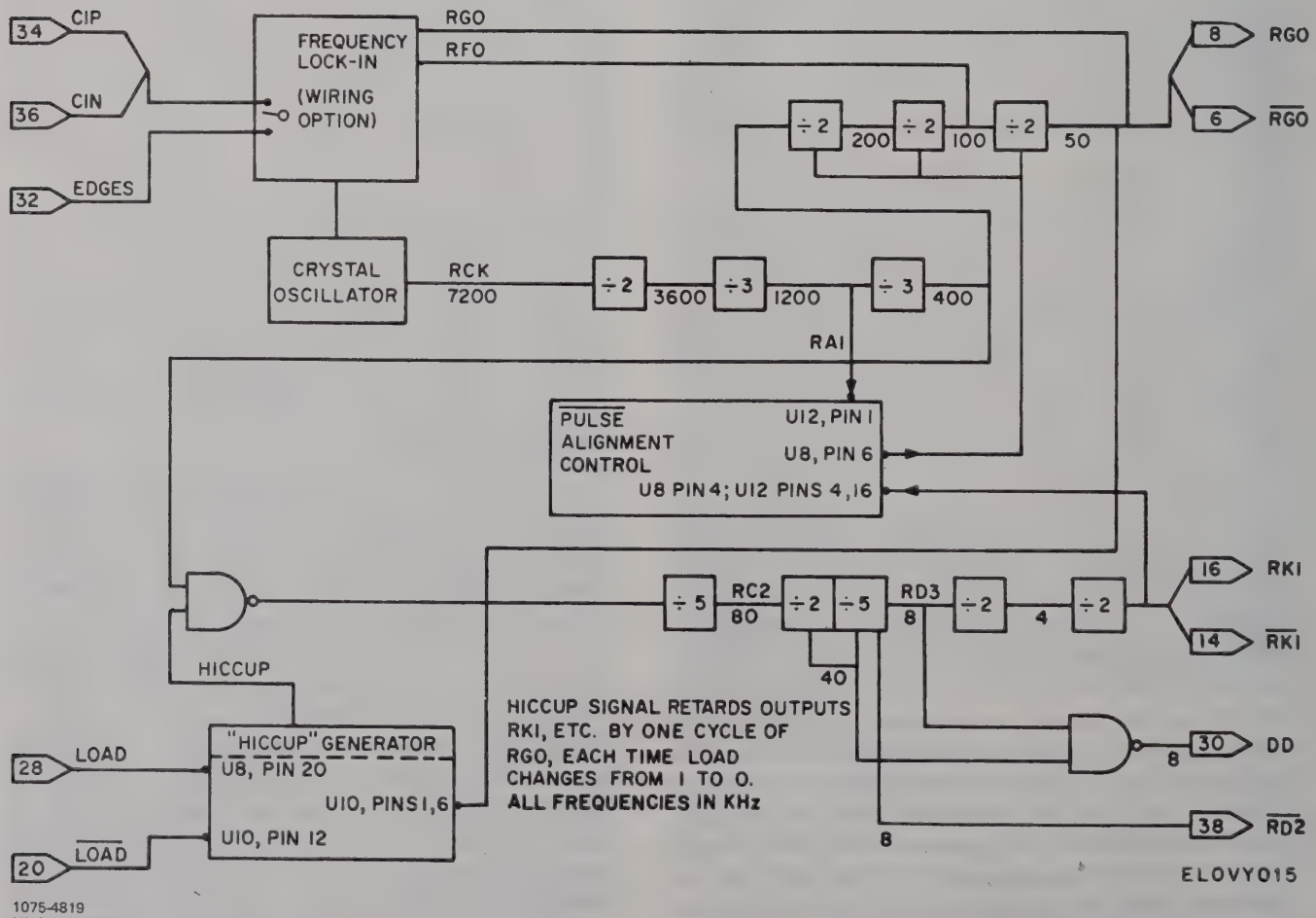


Figure 6-5. Receiver timing board 1A7 block diagram.

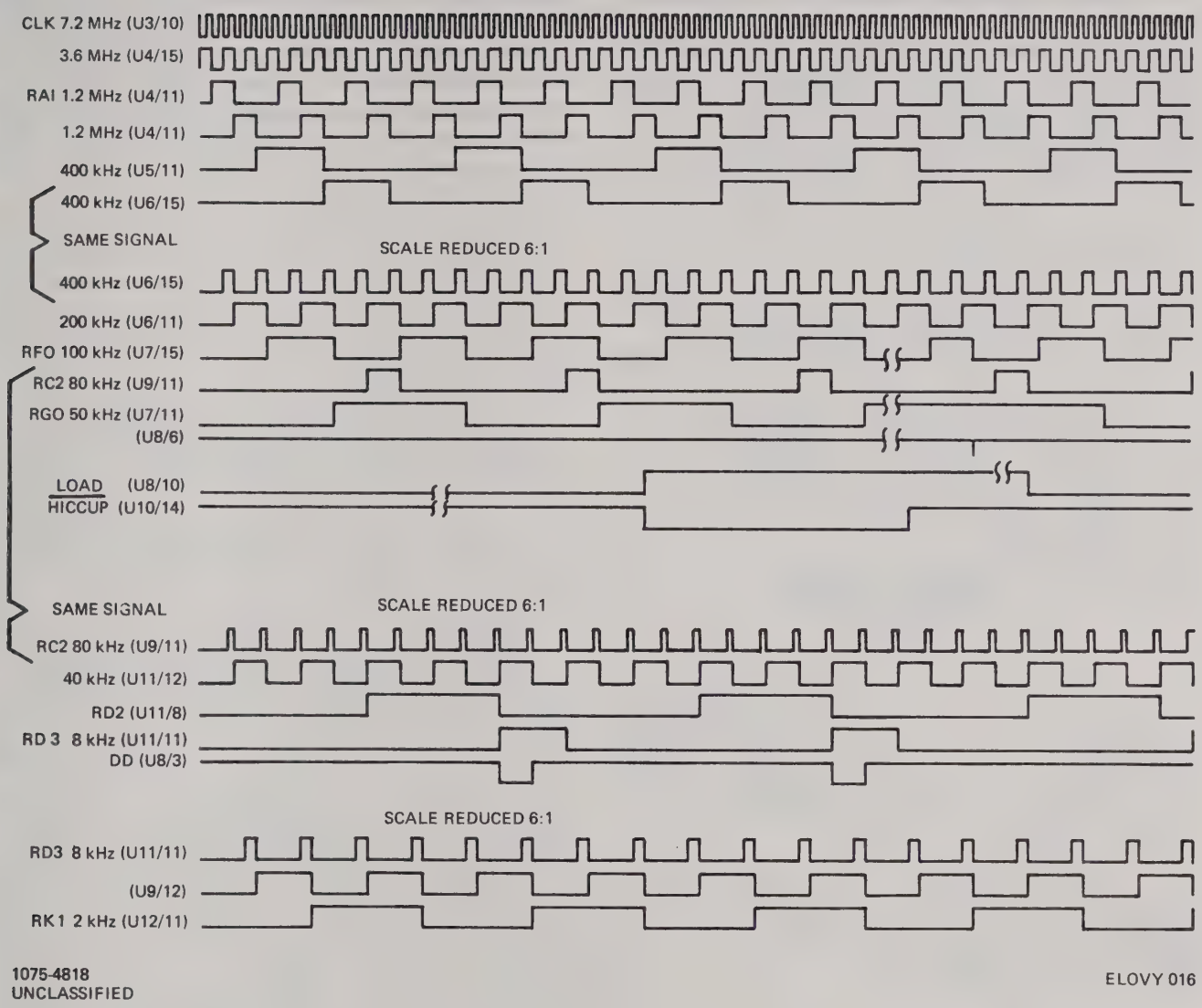


Figure 6-6. Receiver timing board 1A7 waveforms.

(1) The 7.2 MHz crystal oscillator is followed by frequency division steps to 3.6 MHz, and 2 MHz, and 400 kHz. From here there are two frequency-division paths. One divides to frequencies of 200, 100, and 50 kHz; the 50 kHz clock signals RG0 and $\overline{RG0}$ going to connector pins 8 and 6. The other path divides the frequency to 80 kHz (signal RC2), 40 kHz, 8 kHz (signal RD3, duty cycle 20 percent; and, through an inverter, $\overline{RD2}$, duty cycle 60 percent output pin 38) and 2 kHz signals RK1 and $\overline{RK1}$ going to output terminals 16 and 14.

(2) The control of the crystal oscillator frequency, for synchronism with the signals being processed, is accomplished by comparing $\overline{RF0}$ and RG0 (100 kHz and 50 kHz) signals derived from the oscillator with an external signal, either EDGES, derived internally from the signal being processed, or externally supplied clock-input negative signals, CIP and CIN.

(3) The circuit containing flip-flop U12 (with inputs RA1, RK1, and $\overline{RK1}$) and NAND gate U8 is a means of aligning pulses from the two timing chains (400 kHz to 2 kHz, and 400 kHz to 50 kHz).

(4) The circuit with inputs LOAD and $\overline{LOAD}$, with the output $\overline{HICCUP}$ (see glossary) controlling the 400 kHz signal to the timing chain ending at the 2 kHz signals, RK2 and $\overline{RK1}$, is used in conjunction with the sequence detector circuit to vary the selection of bits taken for comparison with the random bit sequence identifying voiceband signals. For detail description, see paragraph 6-7*a*(4).

c. Receiver Sequence Detector Board 1A8 (fig. FO-13 and 6-7).

When the transmitter signal is digitized VOICE, the identifying code in the data stream consists of the bits from the transmitter pseudorandom sequence generator; the code bits are inserted one bit at a time after each group of 24 bits representing the analog input. Thus, starting with a code bit as number 1, the following code bits are 26, 51, 76, 101, ... Since the receiver has no way determining where the code bits are, except by trial and error, the sequence detector will, if necessary, after a study of the string just mentioned, try another series, for example 2, 27, 52, 77, 102, ... Failing here, it will select series 3, 28, 53, 78, 103, ... , and so forth. For convenience in the discussion which follows, these series will be referred to as "bit series 1, series 2, ... ".

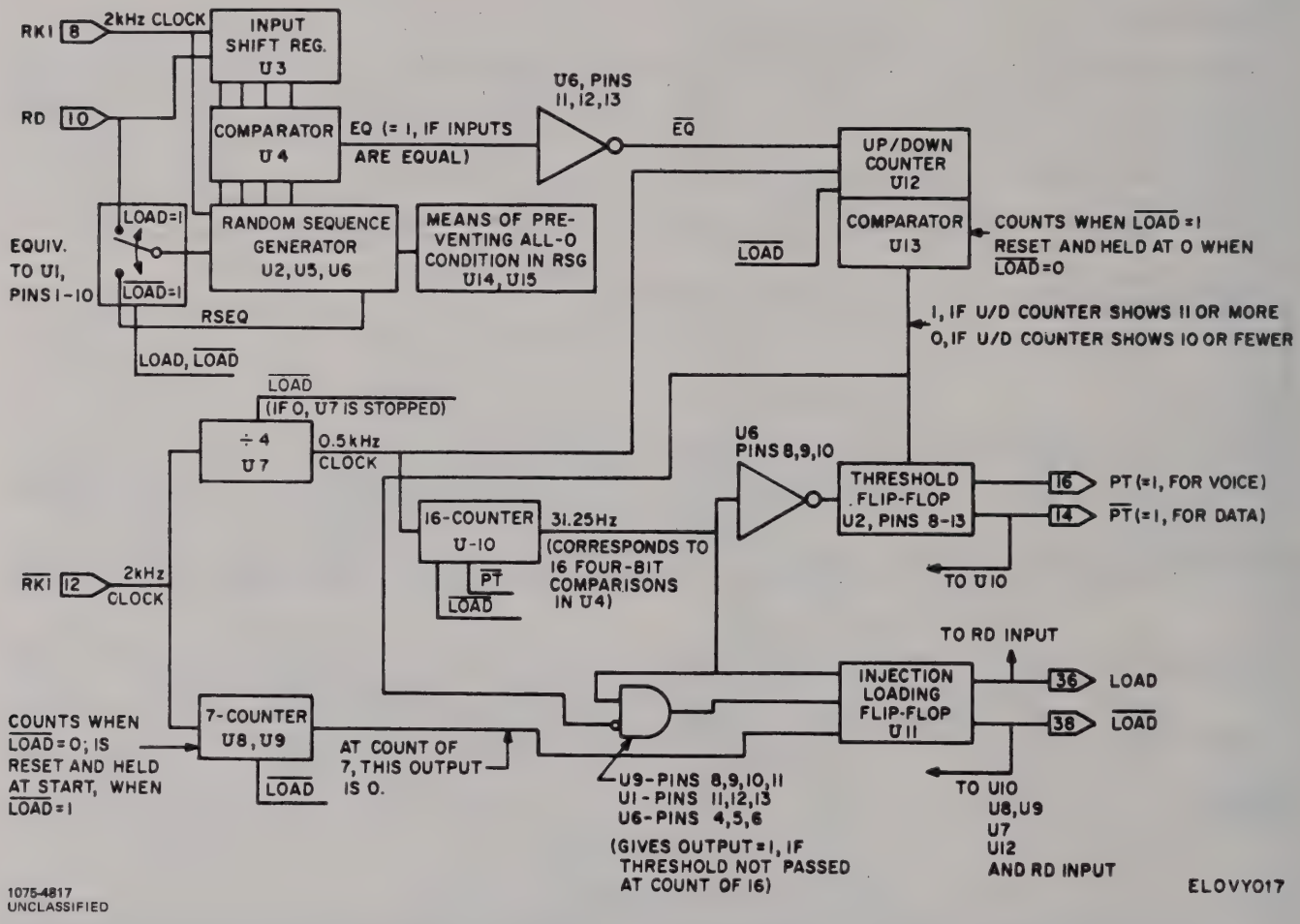


Figure 6-7. Receiver sequence detector board 1A8 block diagram.

NOTE

Because of the clocking of input to the receiver sequence detector board 1A8, all bits not in the series under examination are of no significance and for the present discussion, the phrase "four consecutive bits" means four bits in a series (as just defined), corresponding to a bit count of as many as 100 consecutive bits in the original stream.

(1) Assume a starting condition where the loading-in control signal LOAD equals 1 and the passed threshold signal PT equals 0. A bit series is clocked into the input shift register U3 and into the pseudorandom sequence generator, U2, U5, and U6. The pseudorandom sequence generator is thus injection-loaded in order to get its operation started, and to synchronize it with the incoming data. After seven bits have been clocked in, the 7-counter consisting of U8 and U9 controls the load flip-flop U11 so that LOAD becomes 0, and $\overline{\text{LOAD}}$ becomes 1. The pseudorandom sequence generator becomes self-running, circulating in a pattern derived from the injection-loaded bits, the up/down counter U12 starts counting, and the 7-counter is reset. The two LOAD signals also go the receiver timing board 1A7, and this function will be described later. Of the bits circulating in the pseudorandom sequence generator,

groups of four are compared (in U4) with groups of four of the reclocked data (RD) bits (see not above). The results of the comparison are entered into the u/down counter U12 at a rate of 500 per second by the clock signal from 4-counter flip-flops U7. Because bits in the series under test appear at a two-kHz rate, each entry in U12 represents a comparison of a fresh group of bits (the groups do not overlap).

(2) After 16 such comparisons, 16-counter U10 issues a signal to clock the passed threshold and load flip-flops. If up/down counter U12 shows that 11 or more comparisons indicated agreements, comparator U13 gives a 1 signal to indicate passed threshold. This 1 signal operates flip-flop U2 pins 8 through 13, to give PT equals 1 at pin 9 and PT equals 0 at pin 18. If U13 indicates that the count is too low, the passed threshold flip-flop U2 remains unchanged, and a gate admits the output of register U10 to load flip-flop U11, pin 4. U11 then goes back to its original state, so that new bits from RD are again entering the pseudorandom sequence generator.

(3) This time however the bits, clocked by signal RK1 into U3 and into U5 to reload the sequence generator, are from a different series of bits (para. 6-7*c*). To understand how the series is changed, it is necessary to study a circuit on receiver timing board 1A7. Board 1A7 has a circuit with LOAD and $\overline{\text{LOAD}}$ inputs, and also a 50 kHz clock input RG0. The output $\overline{\text{HICCUP}}$ controls a gate where the 400 kHz is divided to RC2 and eventually to RK1. This circuit produces a single 0 pulse each time LOAD becomes 1, the pulse duration being that of a bit length in the input bit stream RD. The effect is that the timing pulse RK1 is set back one bit, so that bit series 2 is now read in, instead of bit series 1. This process is repeated after every 16 comparisons until the sequence of bits clocked into U3 compares in U4 with the bits of the pseudorandom sequence generator, indicating that the pseudorandom sequence in the incoming data has been found. If no such corresponcence is found, PT and $\overline{\text{PT}}$ remain 0 and 1 respectively, causing indicator lamp RCVR DATA to be lighted and operating appropriate signal gates in receiver filter board 1A9.

(4) If the receiver is operating in voiceband mode, so that LOAD equals 0 and PT equals 1, and the incoming signal becomes a representation of a data stream rather than digitized voiceband, agreement with the pseudorandom sequence no longer occurs. The up/down counting system and the 0.5 kHz clock continue to operate normally, and also the 16-counter U10. However, the output of comparator U13 becomes 0. At the next pulse from the 16-counter, both passed threshold and load flip-flops are reversed, and the original condition is resumed.

(5) A summary of the process of sequence detection is given in the following example:

Ⓐ Assume starting conditions to be PT equals 0, LOAD equals 1. Load 7 bits into pseudorandom sequence generator (injection loading), and into input shift register (bits 1, 2, and 3 are pushed out land lost). After the seven bits are counted, the load flip-flop is reset to LOAD equals 0. This causes the following to occur:

- —Random sequence generator becomes self-running (under clock control).
- —The 0.5 kHz clock starts to count.
- —The 7-counter U8 and U9, used in injection loading, is stopped and reset.
- —The up/down counter U12 is enabled.
- —The 16-counter U10 is started.
- —Groups of four bits (one out of 25) in input bit stream RD are compared with groups of four in the pseudorandom sequence bit stream for 16 attempts. The threshold is 11 or more agreements.

	Threshold not passed	*Threshold passed*
Ⓑ	16-counter reinstates injection loading, with series 2 bits (or series 3, or 4, ... , or 25). Return to Ⓐ	Reloading inhibited. Passed threshold flip-flop goes to voiceband mode. Condition is stable as long as up/down counter remains above threshold. If it drops below return to Ⓑ

- —The HICCUP circuit board 1A7 selects a new series of one out of every 25 bits if threshold is not reached.

(6) The receiver sequence detector board 1A8 has a pulse edge detector circuit entirely independent of the process of sequence detection. It comprises two one-shot pulse generators (U16) and an output gate U9, pins 1, 2, 12, 13. The circuit synchronization pulses (EDGES) at the leading and trailing edges of the incoming data signal ID. These pulses are used to synchronize receiver operation with the incoming signals by slight variation of the oscillator frequency.

d. Receiver Filter Board 1A9. (fig. FO-14). Receiver filter board 1A9 contains a 5-pole active elliptic low-pass filter identical to the one used in transmitter filter board 1A1. It consists of integrated circuits U1, U2, U3, and their associated

resistive and capacitive circuits. Operational amplifier U4 is the voice output amplifier. Two solid state switches are combined in U5 and switch voice or data through the output operational amplifier U7.

(1) The digital-to-analog output signal DAO enters at connector pin 8. After the first filter stage, the signal is brought out on connector pin 6 which is joined externally to connector pin 24 to carry signal RS10 to the second stage. The third stage output goes to output level adjustment R15. The signal divides and one branch feeds the output amplifier U4, whose receiver voice output RVO goes through connector pin 38 to the output transformer T5 and output connector J10 (fig. FO-3). The other branch also goes through the solid state switch U5 to the output amplifier U7. The receiver hybrid output RHO from U7 goes through connector pin 20 to the output transformer T4 and output connector J9.

(2) The reclocked data signal RD enters at connector pin 32, goes through the solid state switch U5 to output amplifier U7, and described for the analog signal in the preceding paragraph.

(3) The solid state switch U5 is controlled by signals PT and PT from receiver sequence detector board 1A8 so that the input of U7 is connected either to the analog signal or to the digital signal, but not both.

CHAPTER 7

DIRECT AND GENERAL SUPPORT MAINTENANCE INSTRUCTIONS

Section I. TROUBLESHOOTING

7-1. Scope of Direct and General Support Maintenance.

a. General. The direct and general support maintenance procedures in this chapter supplement the procedures described in operator and organizational maintenance (ch. 4 and 5). The systematic troubleshooting procedure begins with the operator, is carried through to organizational and reaches a higher category in this chapter. Direct support is based on isolating and replacing faulty parts on the front, center, and rear panels, and replacement of printed wiring boards by using troubleshooting tables and go/no-go procedures. This section gives the tools and test equipment required. Section II lists the troubleshooting procedures, section III describes replacement of parts, and section IV provides checkout and adjustment procedures.

b. Maintenance. Maintenance for the converter is based on the use of troubleshooting tables, the chassis schematic diagram (fig. FO-1), and interconnecting wiring diagrams (fig. FO-4 and FO-5) for performing fault isolation down to a printed wiring board or front, center, and rear panel discrete part level.

7-2. Tools and Test Equipment Required

Table 7-1 lists the tools and test equipment required for maintenance of the converter at direct support.

WARNING

120 vac is present at the rear panel power connector and line filter terminals, the front panel POWER switch and fuse terminals, and the power transformer on the center panel. Serious injury or DEATH may result from contact with these points.

7-3. Organization of Troubleshooting Procedures

a. Much of the troubleshooting of the converter can be performed while the unit remains in the rack. The procedures for checking and replacing the front panel indicator lamps, lampholders and faulty wiring are performed at the operator and organizational categories as detailed in tables 4-3 and 5-3. If the malfunction cannot be resolved by organizational maintenance, and problems with the primary power circuitry are indicated, table 7-2 gives the troubleshooting procedures to be followed. If problems with the power supply are indicated, follow the procedures of table 7-3.

b. The complexity of the converter, and its use as part of an overall communications link, makes it difficult in many cases to determine if the converter is at fault or if there is some other equipment in the link. When it cannot be determined if the converter is at fault from the observations of the operator or from information received from other operators of the communications link, perform the overall converter checks (para 7-9). The voice throughput check (para 7-9*a*), and the data throughput check (para 7-9*b*) will verify converter performance and determine if a malfunction is in the transmitter section or the receiver section. The transmitter section can be checked by performing transmitter data output (bit stream) check (para 7-8*c*).

NOTE

To minimize downtime of an operational unit, replacement of printed wiring boards in sequence can be quickly and easily performed until a more detailed check in accordance with table 7-4 can be made.

c. Troubleshooting to isolate defective printed wiring boards is given in table 7-4. The waveforms referred to in table 7-4 are given in table 7-5. When a defective board is detected, replace it with another from the spare set.

d. To aid troubleshooting of the power supply discrete components and associated circuitry, the chassis schematic diagram, chassis interconnection and the converter interconnection wiring diagrams are provided (fig. FO-1, FO-4 and FO-5).

Table 7-1. Tools and Test Tequipment

Nomenclature designation [a]	Purpose	Qty	National stock No.
Frequency Counter CP-772/U	For testing timing printed wiring boards 1A3 and 1A7.	1	6625-00-922-3586
Multimeter AN/PSM-6B or AN/USM-210	For voltage and continuity testing parts on front, center, and rear panels.	1	6625-00-019-0815
Oscilloscope AN/USM-273	For testing of printed wiring boards.	1	6625-00-930-6637
Audio Signal Generator SG-632/U or O-1025/U.	To simulate the audio or digital input.	2	6625-00-865-9026
Test Accessories Kit [b] Part No. SMB865106 (80063)	To test converter.	1	
Consisting of:			
Test cable, Part No. SMD865108 (80063)	To connect DATA XMTR OUTPUT J5 to DATA RCVR INPUT J8, and CLOCK XMTR OUTPUT J4 to CLOCK RCVR INPUT J7 during testing.	2	
Test cable, Part No. SMC865154 (80063)	To connect XMTR OUTPUT (135 Ω) J12 to RCVR INPUT (135 Ω) J13 during testing.	1	
Terminator, 75 ohm, Part No. SM-C865134 (80063)	To terminate DATA XMTR OUTPUT J5 and CLOCK XMTR OUTPUT with proper load resistor.	2	
Resistor, 620 ohm, ±5%, ½ watt, RCR20G131J.	Dummy load for voice terminal.	1	5905-00-279-1761
Extender board[b], Part No. SMD750075 (80063)	For fault isolation of discrete components on printed wiring boards.	2	
Board extractor[b], Part No. SMC750009 (80063)	For removal of printed wiring board.	1	
Tool Kit, Electronic Equipment TK-105/G	For repair and parts replacement (includes soldering iron).	1	5180-00-610-8177

[a] Or equivalent.
[b] Supplied with each converter.

Table 7-2. Direct and General Support Troubleshooting of Primary Power Circuitry

Malfunction	Probable Cause	Corrective action
1. Power indicator lamp, is not lighted, lamp is known good, and equipment does not operate properly (from table 5-3, step 3).	Defective cable, wiring, or parts in primary power circuit.	Check power cable and connectors, line filter FL1, POWER switch S1, transformer T1, and wiring to power transformer T1. Repair or replace defective parts.
2. One or more mode indicator lamps are not lighted and lamps are known good (from table 5-3, step 6).	*a.* Defective lamp drive circuitry on printed wiring board 1A4 or 1A6.	*a.* Replace printed wiring board 1A4 or 1A6 and verify proper operation by performing paragraph 7-9*a* and *b*.
	b. Defective printed wiring board 1A8.	*b.* Replace printed wiring board 1A8. Continue troubleshooting using table 7-3; and table 7-4 if required.

Table 7-3. Direct and General Support Troubleshooting of Power Supply Circuitry (Center Panel)

Indication of malfunction	Probable cause	Corrective action
1. Indications obtained in paragraph 5-8*b* and table 7-2, item 2, show power supply voltage missing or incorrect at test jack 1A1J1 (+5 vdc transmitter) and/or at test jack 1A6J1 (+5 vdc transmitter) and/or at test jack 1A6J1 (+5 vdc receiver).	NOTE If +5 vdc is missing or incorrect at both test jacks, probable cause is common to both supplies and in circuitry preceding voltage regulators U1 and U2 (fig. FO-1 and FO-4). If only one +5 vdc is missing or incorrect, probable cause is in regulators U1 or	

Table 7-3. Direct and General Support Troubleshooting of Power Supply Circuitry (Center Panel)— Continued

Indication of malfunction	Probable cause	Corrective action
	U2, or parts and wiring following the regulator in the defective supply.	
	a. Shorted circuitry on printed wiring board.	*a.* While monitoring 1A1J1 and/or 1A6J1 with multimeter, remove printed wiring boards one at a time. Replace defective board. If problem is not corrected, proceed to *b* below.
	b. Defective wiring.	*b.* Refer to paragraph 7-6*c* for access to center panel. Check wiring between center panel, 1A10 and 1A11. If correct, go to *c* below.
	c. Defective U1 and/or U2.	*c.* Check input voltage to U1 and U2 (12 ± 2 vdc). If voltage is correct, replace U1 and/or U2. If voltage is not correct, go to *d* below.
	d. Defective capacitor.	*d.* Disconnect wire to terminal E3 and check capacitors C1, C2, C3, and C6 for short or open. If capacitors are all good, go to *e* below.
	e. Defective transformer.	*e.* Check transformer T1 winding 3-4 for proper voltage (11 ± 2 vac). If incorrect, replace transformer. If correct, go to *f* below.
	f. Defective diodes.	*f.* Check diodes CR1 through CR4 for short or open. Replace defective diode. Reconnect wiring as required.
2. Power supply voltage missing or incorrect at test jack 1A1J2 (+15 vdc).	*a.* Shorted circuitry on printed wiring board.	*a.* While monitoring A1A1J2, remove printed wiring boards 1A1 through 1A9, one at a time. Replace defective board if this is the cause. If not, go to *b* below.
	b. Defective wiring.	*b.* Check wiring between center panel, 1A10 and 1A11. If correct, go to *c* below.
	c. Defective U3.	*c.* Check input voltage to U3 (29 ± 3 vdc). If correct, replace U3. If not correct, go to *d* below.
	d. Defective capacitor.	*d.* Disconnect wire to terminal E7 and check capacitors C7 and C8 for short or open. If capacitors are good, go to *e* below.
	e. Defective transformer.	*e.* Check transformer T1 winding 5-6 for proper voltage (28 ± 3 vac). If incorrect, replace transformer. If correct, go to *f* below.
	f. Defective diodes.	*f.* Check diodes CR5 through CR8 for short or open. Replace, defective diode. Reconnect wiring as required.
3. Power supply voltage missing or incorrect at test jack 1A1J8 (−15 vdc).	*a.* Shorted circuitry on printed wiring board.	*a.* While monitoring 1A1J8, remove printed wiring boards 1A1 through 1A9, one at a time. Replace defective board if this is the cause. If not, go to *b* below.
	b. Defective wiring.	*b.* Check wiring between center panel, 1A10 and 1A11. If correct, go to *c* below.
	c. Defective U4.	*c.* Check input voltage to U4 (−15 ± 2 vdc). If correct, replace U4. If not correct, go to *d* below.

Table 7-3. Direct and General Support Troubleshooting of Power Supply Circuitry (Center Panel)— Continued

Indication of malfunction	Probable cause	Corrective action
3. (Continued)	*d.* Defective capacitor.	*d.* Disconnect wire to terminal E11 and check capacitors C9 and C10 for short or open. If capacitors are all good, go to *e* below.
	e. Defective transformer.	*e.* Check transformer T1 winding 7-8 for proper voltage (28 ± 3 vac). If incorrect, replace transformer. If correct, go to *f* below.
	f. Defective diode.	*f.* Check diodes CR9 thru CR12 for short or open. Replace defective diode. Reconnect wiring as required.

Table 7-4. Direct and General Support Troubleshooting to Isolate Defective Printed Boards Input/Output Line Transformers and Front Panel Mode Switch

NOTE

Oscilloscope conditions are listed next to waveforms in table 7-5.

Step No.	Malfunction	Procedure	Indication	Corrective Action or Comment
1	The voice throughput check (para 7-9*a*) indicates the converter does not operate properly in voice throughput mode. **NOTE** The voice throughput check is made with cable SMD865108 connecting J5 to J8, and also repeated with cable SM-C865154 connecting J12 to J13. If in both cases the converter does not operate properly, start procedure at *a* above. If voice throughout mode operates properly with cable SMD865108 and does not operate properly with cable SMC865154, start procedure at *ap* below.	*a*. Open front panel. Monitor test jack 1A2J3 with oscilloscope. See waveform 1.	*a*. (1) Correct signal. (2) Incorrect signal.	*a*. (1) Continue 1*b* below. (2) Continue 1*o* below.
		b. Monitor test jack 1A1J6. See waveform 2.	*b*. (1) Correct signal. (2) Incorrect signal.	*b*. (1) Continue 1*c* below. (2) Continue 1*r* below.
		c. Monitor test jack 1A2J1. See waveform 3.	*c*. (1) Correct signal. (2) Incorrect signal.	*c*. (1) Continue 1*d* below. (2) Continue 1*s* below.
		d. Monitor test jack 1A2J2. See waveform 4.	*d*. (1) Correct signal. (2) Incorrect signal.	*d*. (1) Continue 1*e* below. (2) Continue 1*v* below.
		e. Monitor test jack 1A2J4. See waveform 5.	*e*. (1) Correct signal. (2) Incorrect signal.	*e*. (1) Continue 1*f* below. (2) Continue 1*t* below.
		f. Monitor test jack 1A2J5. See waveform 6.	*f*. (1) Correct signal. (2) Incorrect signal.	*f*. (1) Continue 1*g* below. (2) Continue 1*aa* below.
		g. Monitor test jack 1A4J6. See waveform 7.	*g*. (1) Correct signal (2) Incorrect signal.	*g*. (1) Continue 1*h* below. (2) Continue 1*ad* below.
		h. Monitor test jack 1A5J3. See waveform 8.	*h*. (1) Incorrect signal. (2) Incorrect signal.	*h*. (1) Continue 1*i* below. (2) Continue 1*ae* below.
		i. Monitor test jack 1A5J4. See waveform 8.	*i*. (1) Correct signal. (2) Incorrect signal.	*i*. (1) Continue 1*j* below. (2) Continue 1*ag* below.
		j. Monitor test jack 1A6J2. See waveform 9.	*j*. (1) Correct signal. (2) Incorrect signal.	*j*. (1) Continue 1*ai* below. (2) Continue 1*ai* below.
		k. Monitor test jack 1A6J4. See waveform 10.	*k*. (1) Correct signal. (2) Incorrect signal.	*k*. (1) Continue 1*l* below. (2) Continue 1*al* below.
		l. Monitor test jack 1A6J3. See waveform 11.	*l*. (1) Correct signal. (2) Incorrect signal.	*l*. (1) Continue 1*m* below. (2) Continue 1*am* below.
		m. Remove and replace printed wiring board 1A9 and check converter for voice throughput, paragraph 7-9*a*.	*m*. (1) Correct output. (2) Incorrect output.	*m*. (1) Restore unit to normal operation. (2) Continue 1*n* below.
		n. Remove printed wiring board 1A9 and replace original 1A9. Remove top cover and center panel. Check transformer T5 and wiring to and from T5. Replace T5 if defective and/or repair wiring. Check converter for voice throughput.	*n*. (1) Correct output. (2) Incorrect output.	*n*. (1) Restore unit to normal operation. (2) Arrange for troubleshooting and repair at depot maintenance.
		o. Monitor voice input signal at rotary switch S2, deck B, pin 1. See waveform 1.	*o*. (1) Correct signal. (2) Incorrect signal.	*o*. (1) Continue 1*p* below. (2) Continue 1*q* below.
		p. Remove and replace rotary switch S2 and resistor R1. Check converter for voice throughput.	*p*. (1) Correct output. (2) Incorrect output.	*p*. (1) Restore unit to normal operation. (2) Continue 1*q* below.
		q. Remove top cover and center panel. Check T3 and replace if	*q*. (1) Correct output.	*q*. (1) Restore unit to normal operation.

Table 7-4. Direct and General Support Troubleshooting to Isolate Defective Printed Wiring Boards, Input/Output Line Transformers and Front Panel Mode Switch—Continued

Step No.	Malfunction	Procedure	Indication	Corrective Action or Comment
1. (Continued)		necessary. Replace center panel and top cover. Check converter for voice throughput.	(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		r. Remove and replace printed wiring board 1A1. Check converter for voice throughput.	*r.* (1) Correct output.	*r.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		s. Monitor test jack 1A3J7. See waveform 12.	*s.* (1) Correct signal.	*s.* (1) Continue 1*t* below.
			(2) Incorrect signal.	(2) Continue 1*u* below.
		t. Remove and replace printed wiring board 1A2. Check converter for voice throughput.	*t.* (1) Correct output.	*t.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Continue 1*u* below.
		u. Remove and replace printed wiring board 1A3. Check converter for voice throughput.	*u.* (1) Correct output.	*u.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		v. Monitor test jack. 1A3J5. See waveform 13.	*v.* (1) Correct signal.	*v.* Continue 1*w* below.
			(2) Incorrect signal.	Continue 1*x* below.
		w. Remove and replace printed wiring board 1A2. Check converter for voice throughput.	*w.* (1) Correct signal.	*w.* (1) Restore unit to normal operation.
			(2) Incorrect signal.	(2) Continue 1*y* below.
		x. Remove and replace printed wiring board 1A3. Check converter for voice throughput.	*x.* (1) Correct output.	*x.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		y. Remove printed wiring board 1A2 and replace original 1A2. Remove and replace board 1A3. Check converter for voice throughput.	*y.* (1) Correct output.	*y.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		aa. Monitor test jack 1A3J6. See waveform 14.	*aa.* (1) Correct signal.	*aa.* (1) Continue 1*ab* below.
			(2) Incorrect signal.	(2) Continue 1*ac* below.
		ab. Remove and replace printed wiring board 1A3. Check converter for voice throughput.	*ab.* (1) Correct output.	*ab.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Continue 1*ac* below.
		ac. Remove and replace printed wiring board 1A2. Check converter for voice throughput.	*ac.* (1) Correct output.	*ac.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		ad. Remove and replace printed wiring board 1A4. Check converter for voice throughput.	*ad.* (1) Correct output.	*ad.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		ae. Remove and replace printed wiring board 1A4. Check converter for voice throughput.	*ae.* Correct output.	*ae.* (1) Restore unit to normal operation.
			Incorrect output.	(1) Continue 1*af* below.

Table 7-4. Direct and General Support Troubleshooting to Isolate Defective Printed Wiring Boards, Input/Output Line Transformers and Front Panel Mode Switch—Continued

Step No.	Malfunction	Procedure	Indication	Corrective Action or Comment
1. (Continued)		*af.* Remove printed wiring board 1A4 and replace original 1A4. Remove and replace board 1A5. Check converter for voice throughput.	*af.* (1) Correct output.	*af.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		ag. Remove and replace printed wiring board 1A4. Check converter for voice throughput.	*ag.* (1) Correct output.	*ag.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Continue *ah* below.
		ah. Remove board 1A4 and replace original 1A4. Remove and replace 1A5. Check converter for voice throughput.	*ah.* (1) Correct output.	*ah.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		ai. Monitor test jack 1A7J6. See waveform 15.	*ai.* (1) Correct signal.	*ai.* (1) Continue 1*aj* below.
			(2) Incorrect signal.	(2) Continue 1*ak*.
		aj. Remove and replace board 1A6. Check converter for voice throughput.	*aj.* (1) Correct signal.	*aj.* (1) Restore unit to normal operation.
			(2) Incorrect signal.	(2) Arrange for troubleshooting and repair at depot maintenance.
		ak. Remove and replace board 1A6. Check converter for voice throughput.	*ak.* (1) Correct output.	*ak.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		al. Remove and replace board 1A6. Check converter for voice throughput.	*al.* (1) Correct output.	*al.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		am. Remove and replace board 1A6. Check converter for voice throughput.	*am.* (1) Correct output.	*am.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Continue 1*an* below.
		an. Remove board 1A6 and replace with original 1A6. Remove and replace board 1A8. Check converter for voice throughput.	*an.* (1) Correct output.	*an.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Continue 1*ao* below.
		ao. Remove board 1A8 and replace with original 1A8. Remove and replace board 1A7. Check converter for voice throughput.	*ao.* (1) Correct output.	*ao.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		ap. Remove cable SMD865108 and place 75 ohms terminator (table 7-1), on connector J5 Remove cable SMC865154 and connect 130 ohms resistor (table 7-1), to terminals 1 and 2 of J12. Connect J12 terminal 2 to ground. Connect oscilloscope input A to J12 terminal 1. Verify waveform shown in table 7-7 (waveform 3).	*ap.* (1) Correct signal.	*ap.* (1) Continue 1*ar* below.
			(2) Incorrect signal.	(2) Continue 1*aq* below.

Table 7-4. Direct and General Support Troubleshooting to Isolate Defective Printed Wiring Boards, Input/Ouput Line Transformers and Front Panel Mode Switch—Continued

Step No.	Malfunction	Procedure	Indication	Corrective Action or Comment
1. (Continued)		*aq.* Remove and replace board 1A5, recheck waveform of *ap* above.	*aq.* (1) Correct signal.	*aq.* (1) Restore unit to normal operation.
			(2) Incorrect signal.	(2) Continue 1*as* below.
		ar. Check cable SMC865154 for continuity, repair or replace if defective. Remove the 130 ohms resistor from J12 and connect known good cable SMC865154 between J12 and J13. Check converter for voice throughput.	*ar.* (1) Correct output.	*ar.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Continue 1*at* below.
		as. Remove rear top cover and check T6. Replace if necessary. Check converter for voice throughput.	*as.* (1) Correct output.	*as.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Arrange for troubleshooting and repair at depot maintenance.
		at. Remove and replace board 1A6. Check converter for voice throughput.	*at.* (1) Correct output.	*at.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Continue 1*au* below.
		au. Remove rear top cover and check T7. Replace if necessary. Check converter for voice throughput.	*au.* (1) Correct output.	*au.* (1) Restore unit to normal operation.
			(2) Incorrect output.	(2) Continue 1*av* below.
		av. Remove board 1A6 and replace with original 1A6. Replace rear top cover and close front panel.	*av.* None	*av.* Arrange for troubleshooting and repair at depot maintenance.
2	The data throughput check (para 7-9*b*) indicates the converter does not operate properly in the data throughput mode.	*a.* Open front panel. Monitor test jacks 1A5J3. 1A5J4. See waveform 8.	*a.* (1) Correct signal.	*a.* (1) Continue 2*b* below.
			(2) Incorrect signal.	(2) Continue 2*g* below.
	NOTE The data throughput check is made with cable SMD865108 connecting J5 to J8, and also repeated with cable SMC865154 connecting J12 to J13. If in both cases the converter does not operate properly, start procedure at 2*a*. If data throughput mode operates properly with cable SMD865108 and does not operate properly with cable SMC865154, follow procedures of 1*ap* through 1*av* above.	*b.* Monitor test jack 1A6J2. See waveform 9.	*b.* (1) Correct signal.	*b.* (1) Continue 2*c* below.
			(2) Incorrect signal.	(2) Continue 2*m* below.
		c. Monitor test jack 1A6J4. See waveform 10.	*c.* (1) Correct signal.	*c.* (1) Continue 2*d* below.
			(2) Incorrect signal.	(2) Continue 2*o* below.
		d. Monitor test jack 1A9J7. See waveform 16.	*d.* (1) Correct signal.	*d.* (1) Continue 2*e* below.
			(2) Incorrect signal.	(2) Continue 2*p* below.
		e. Monitor output signal at terminal 1 of rear panel connector J9.	*e.* (1) Converter hybrid output correct (approximate 0.8 Vp-p squarewave).	*e.* (1) Continue 2*g* below.
			(2) Incorrect hybrid output.	(2) Continue 2*f* below.
		f. Check transformer T4 and wiring to and from transformer T4. Replace T4 if defective and/or repair wiring. Check converter for data throughput.	*f.* (1) Correct data throughput.	*f.* (1) Restore unit to normal operation.
			(2) Incorrect data throughput.	(2) Continue 2*g* below.
		g. Monitor test jack 1A1J3. See waveform 1.	*g.* (1) Correct signal.	*g.* (1) Continue 2*h* below.
			(2) Incorrect signal.	(2) Continue 2*q* below.
		h. Monitor test jack 1A4J4. See waveform 17.	*h.* (1) Correct signal.	*h.* (1) Continue 2*i* below.
			(2) Incorrect signal.	(2) Continue 2*j* below.

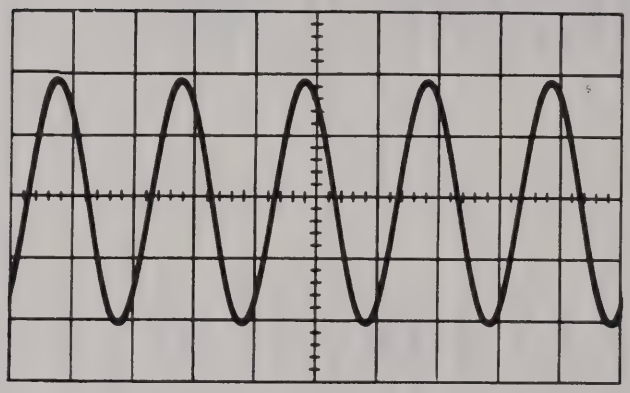
Table 7-4. Direct and General Support Troubleshooting to Isolate Defective Printed Wiring Boards, Input/Output Line Transformers and Front Panel Mode Switch—Continued

Step No.	Malfunction	Procedure	Indication	Corrective Action or Comment
2. (Continued)		*i.* Remove and replace board 1A5. Check converter for data throughput.	*i.* (1) Correct output. (2) Incorrect output.	*i.* (1) Restore unit to normal operation. (2) Continue 2*j* below.
		j. Monitor test jack 1A3J6. See waveform 14.	*j.* (1) Correct signal. (2) Incorrect signal.	*j.* (1) Continue 2*k* below. (2) Continue 2*l* below.
		k. Remove and replace 1A4. Check converter for data throughput.	*k.* (1) Correct output. (2) Incorrect output.	*k.* (1) Restore unit to normal operation. (2) Continue 1 below.
		l. Remove and replace 1A3. Check converter for data throughput.	*l.* (1) Correct output. (2) Incorrect output.	*l.* (1) Restore unit to normal operation. (2) Arrange for troubleshooting and repair shooting and repair at depot maintenance.
		m. Monitor test jack 1A7J6. See waveform 15.	*m.* (1) Correct signal. (2) Incorrect output.	*m.* (1) Continue 2*n* below. (2) Continue 2*o* below.
		n. Remove and replace board 1A6. Check converter for data throughput.	*n.* (1) Correct output. (2) Incorrect output.	*n.* (1) Restore unit to normal operation. (2) Arrange for troubleshooting and repair at depot maintenance.
		o. Remove and replace board 1A7. Check converter for data throughput.	*o.* (1) Correct output. (2) Incorrect output.	*o.* (1) Restore unit to normal operation. (2) Arrange for troubleshooting and repair at depot maintenance.
		p. Remove and replace 1A9. Check converter for data throughput.	*p.* (1) Correct output. (2) Incorrect output.	*p.* (1) Restore unit to normal operation. (2) Arrange for troubleshooting and repair at depot maintenance.
		q. Monitor rotary switch S2, deck B, pin 3. Waveform will be the same as at hybrid input receptacle 1J3.	*q.* (1) Correct signal. (2) Incorrect signal.	*q.* (1) Continue 2*r* below. (2) Continue 2*s* below.
		r. Remove and replace switch S2 and resistor R1. Check converter for data throughput.	*r.* (1) Correct output. (2) Incorrect output.	*r.* (1) Restore unit to normal operation. (2) Continue 2*s* below.
		s. Remove top cover and center panel. Check transformer T2, replace if necessary. Check converter for data throughput. Close front panel.	*s.* (1) Correct output. (2) Incorrect output.	*s.* (1) Restore unit to normal operation. (2) Arrange for troubleshooting and repair at depot maintenance.

Table 7-5. Waveforms (1 thru 17) for Troubleshooting Converter
(Sheet 1 of 6)

WAVEFORM 1

1A1J3



VERTICAL		HORIZONTAL	
SENS.	0.5/DIV	SWEEP	0.5 mS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	AC

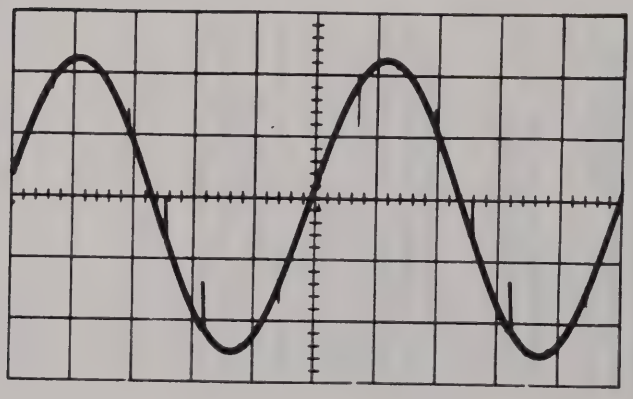
UNIT SETUP

POSITION OF S2 HIGH LEVEL VOICE

INPUT SIGNAL 1 kHz, 0 dBm

WAVEFORM 2

1A1J6



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	0.2 mS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	SINGLE SWEEP
		SLOPE	+
		COUPLING	DC

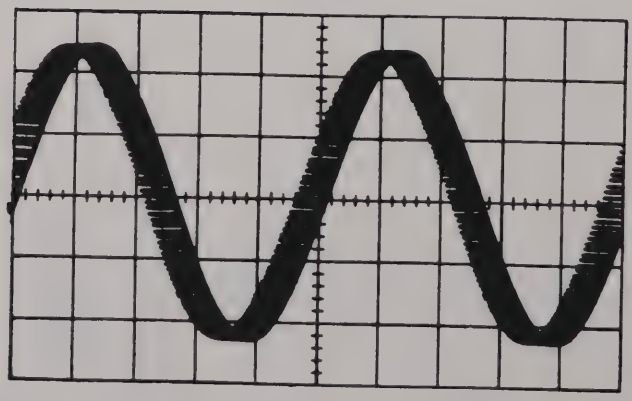
UNIT SETUP

POSITION OF S2 HIGH LEVEL VOICE

INPUT SIGNAL 1 kHz, 0 dBm

WAVEFORM 3

1A2J1



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	0.2m S/DIV
COUPLING	DC	SYNC SOURCE	EXT
MODE	CH1	SYNC FROM	1A1J3
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	DC

UNIT SETUP

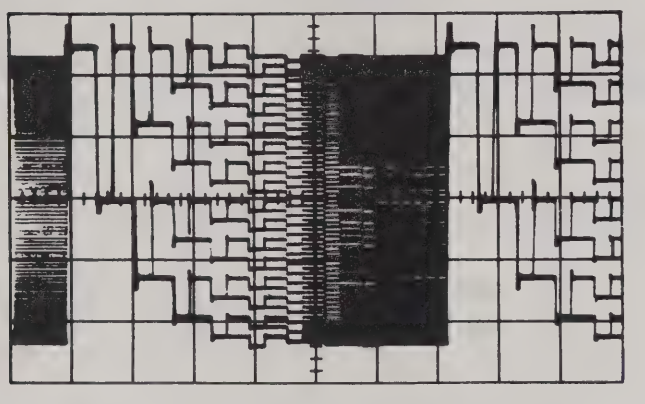
POSITION OF S2 HIGH LEVEL VOICE

INPUT SIGNAL 1 kHz, 0 dBm

Table 7-5. Waveforms (1 thru 17) **for Troubleshooting Converter - Continued**
(Sheet 2 of 6)

WAVEFORM 4

1A2J2



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	20 µS/DIV
COUPLING	DC	SYNC SOURCE	EXT
MODE	CH1	SYNC FROM	1A3J7
		SYNC MODE	NORM
		SLOPE	
		COUPLING	LFREJ

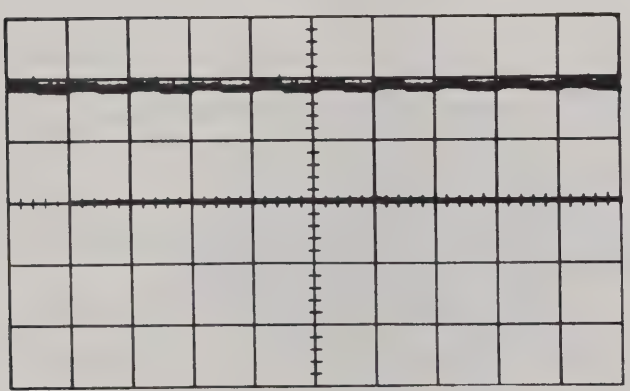
UNIT SETUP

POSITION OF S2 HIGH LEVEL VOICE

INPUT SIGNAL 1 kHz, 0 dBm

WAVEFORM 5

1A2J4



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	0.5 mS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

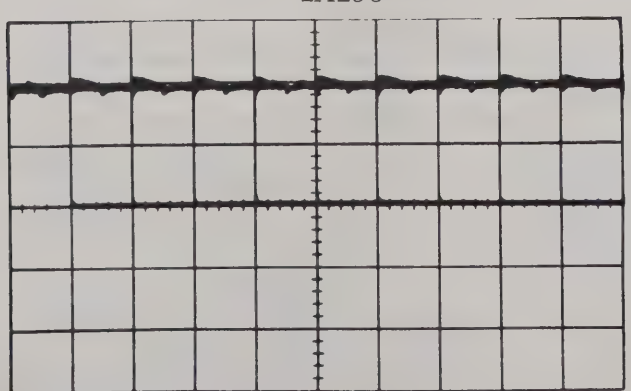
UNIT SETUP

POSITION OF S2 HIGH LEVEL VOICE

INPUT SIGNAL 1 kHz, 0 dBm

WAVEFORM 6

1A2J5



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	20 µS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

UNIT SETUP

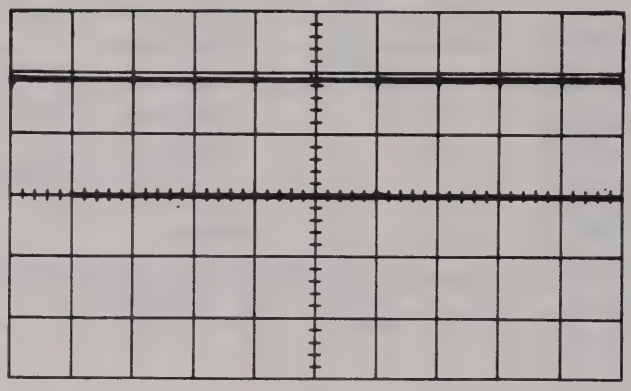
POSITION OF S2 HIGH LEVEL VOICE

INPUT SIGNAL 1 kHz, 0 dBm

Table 7-5. Waveforms (1 thru 17) **for Troubleshooting Converter - Continued**
(Sheet 3 of 6)

WAVEFORM 7

1A4J6



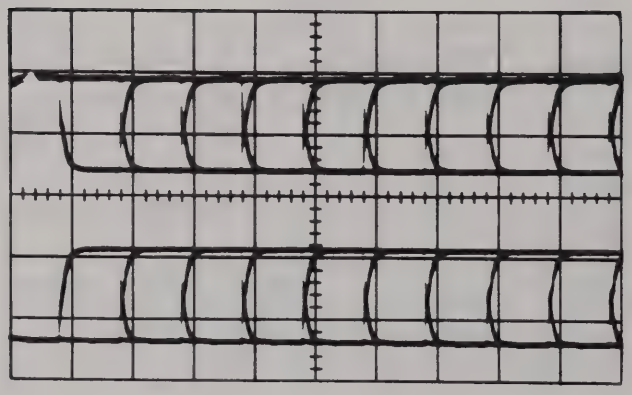
VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	20 µS/SEC
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

UNIT SETUP

POSITION OF S2 HIGH LEVEL VOICE
INPUT SIGNAL 1 kHz, 0 dBm

WAVEFORM 8

1A5J3 AND 1A5J4



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	20 µS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	ALT	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

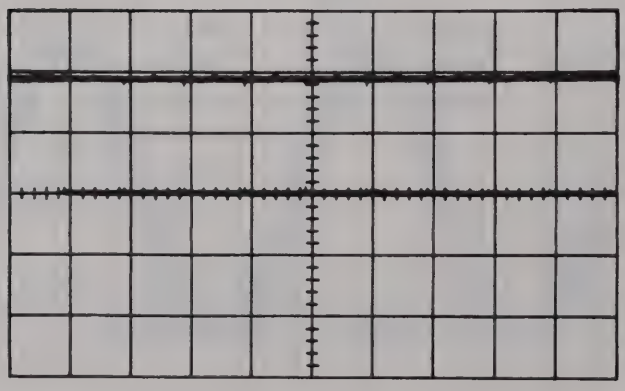
UNIT SETUP

POSITION OF S2 HIGH LEVEL VOICE
INPUT SIGNAL 1 kHz, 0 dBm

Note: Connect 75-ohm terminator (SMC865134) at DATA XMTR OUTPUT J5.

WAVEFORM 9

1A6J2



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	20 µS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	HFREJ

UNIT SETUP

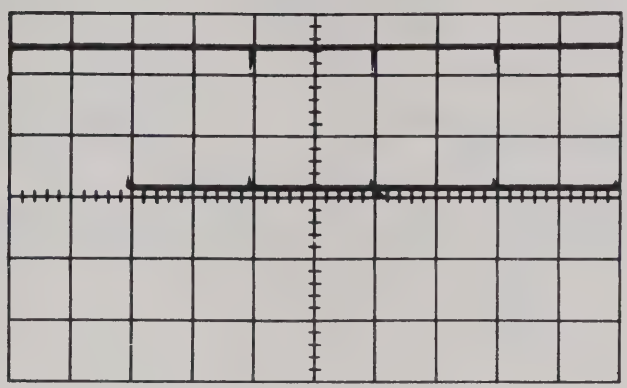
POSITION OF S2 HIGH LEVEL VOICE
INPUT SIGNAL 1 kHz, 0 dBm

Note: DATA XMTR OUTPUT J5 connected to DATA RCVR INPUT J8.

Table 7-5. Waveforms (1 thru 17) **for Troubleshooting Converter - Continued**
(Sheet 4 of 6)

WAVEFORM 10

1A6J4



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	10 µS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

UNIT SETUP

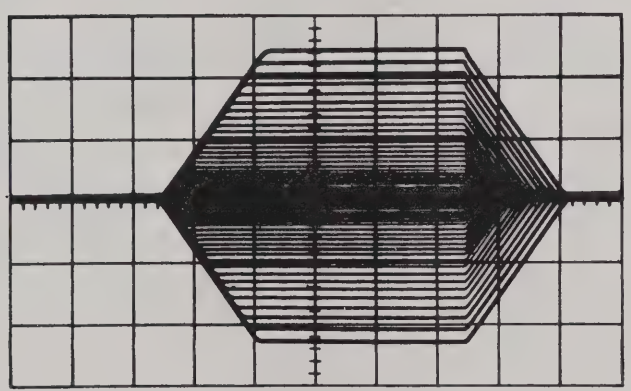
POSITION OF S2: HIGH LEVEL VOICE

INPUT SIGNAL: 1 kHz, 0 dBm

Note: DATA XMTR OUTPUT J5 connected to DATA RCVR INPUT J8.

WAVEFORM 11

1A6J3



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	10 µS/DIV
COUPLING	DC	SYNC SOURCE	EXT
MODE	CH1	SYNC FROM	1A7J5
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

UNIT SETUP

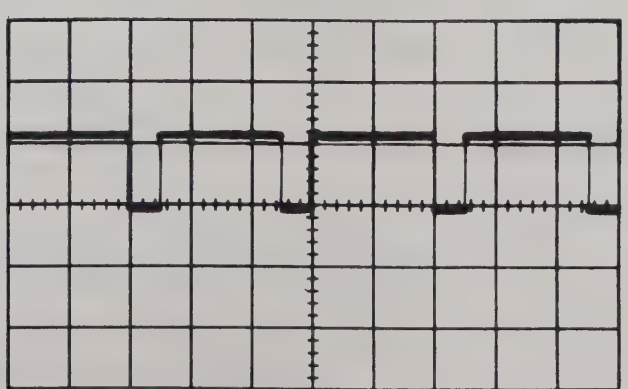
POSITION OF S2: HIGH LEVEL VOICE

INPUT SIGNAL: 1 kHz, 0 dBm

Note: DATA XMTR OUTPUT J5 connected to DATA RCVR INPUT J8.

WAVEFORM 12

1A3J7



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	50 µS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

UNIT SETUP

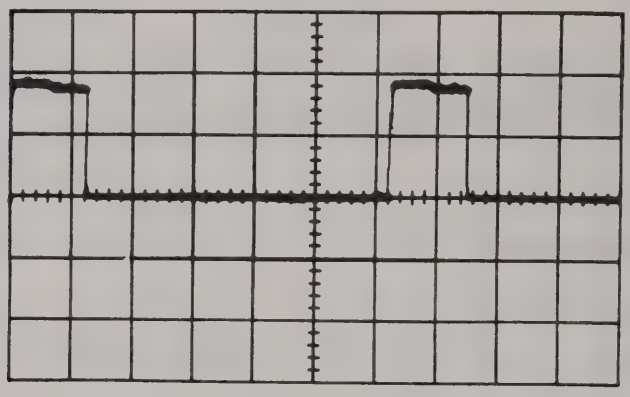
POSITION OF S2: HIGH LEVEL VOICE

INPUT SIGNAL: 1 kHz, 0 dBm

Table 7-5. Waveforms (1 thru 17) **for Troubleshooting Converter** - Continued
(Sheet 5 of 6)

WAVEFORM 13

1A3J5



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	20 µS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	NORM
		SYNC MODE	
		SLOPE	+
		COUPLING	LFREJ

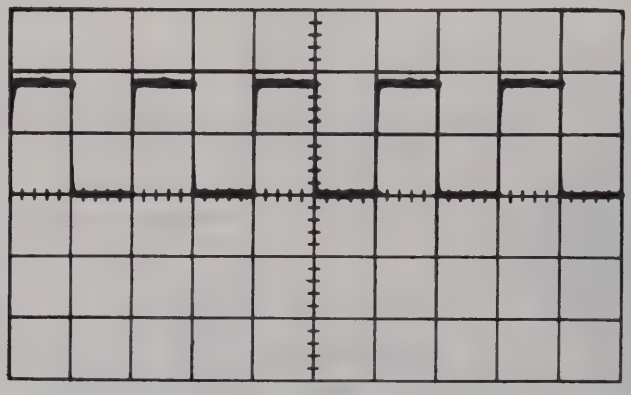
UNIT SETUP

POSITION OF S2 HIGH LEVEL VOICE

INPUT SIGNAL 1 kHz, 0 dBm

WAVEFORM 14

1A3J6



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	10 µS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

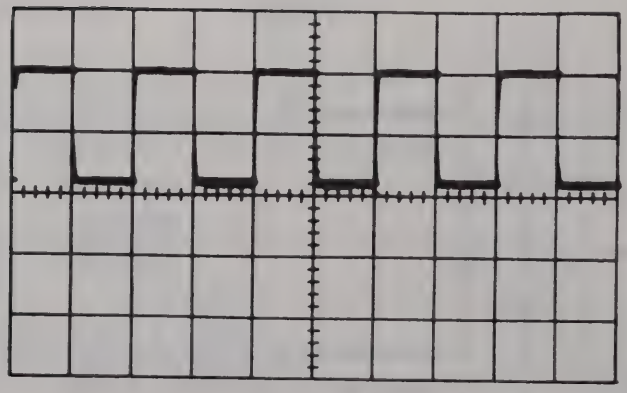
UNIT SETUP

POSITION OF S2 HIGH LEVEL VOICE

INPUT SIGNAL 1 kHz, 0 dBm

WAVEFORM 15

1A7J6



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	10 µS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

UNIT SETUP

POSITION OF S2 HIGH LEVEL VOICE

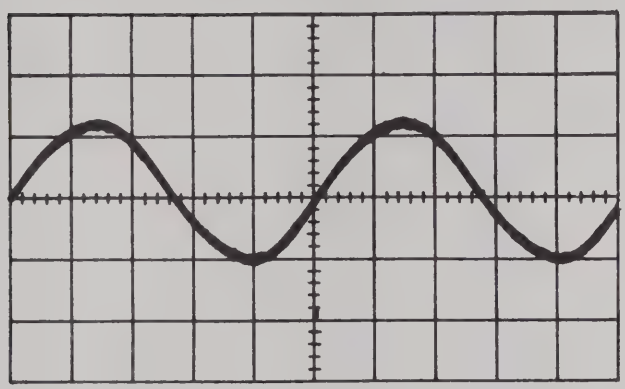
INPUT SIGNAL 1 kHz, 0 dBm

Note: DATA XMTR OUTPUT J5 connected to DATA RCVR INPUT J8.

Table 7-5. Waveforms (1 thru 17) **for Troubleshooting Converter - Continued**
(Sheet 6 of 6)

WAVEFORM 16

1A9J7



VERTICAL		HORIZONTAL	
SENS.	1 V/DIV	SWEEP	0.2 mS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	HFREJ

UNIT SETUP

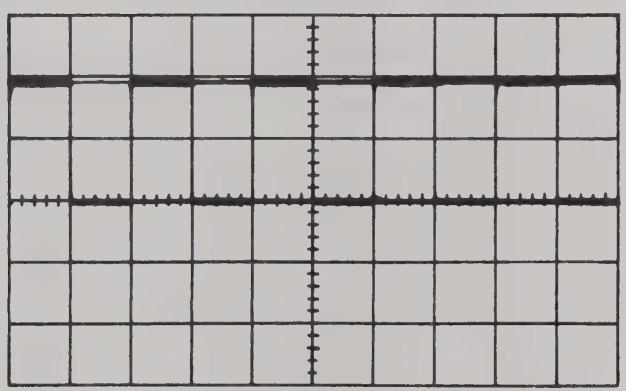
POSITION OF S2 HIGH LEVEL VOICE

INPUT SIGNAL 1 kHz, 0 dBm

Note: DATA XMTR OUTPUT J5 connected to DATA RCVR INPUT J8.

WAVEFORM 17

1A4J4



VERTICAL		HORIZONTAL	
SENS.	2 V/DIV	SWEEP	20 µS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

UNIT SETUP

POSITION OF S2 HYBRID

INPUT SIGNAL 25 kHz, 1 Vrms

Section II. MAINTENANCE OF CONVERTER

7-4. General

Maintenance instructions in this section support necessary repairs required to support troubleshooting in section II. Removal and replacement of parts on the front and rear panels, and replacement of printed wiring boards, can be accomplished without removing the unit from the rack. The unit must be removed from the rack for removal and replacement of parts on the center and rear panels (fig. 7-1).

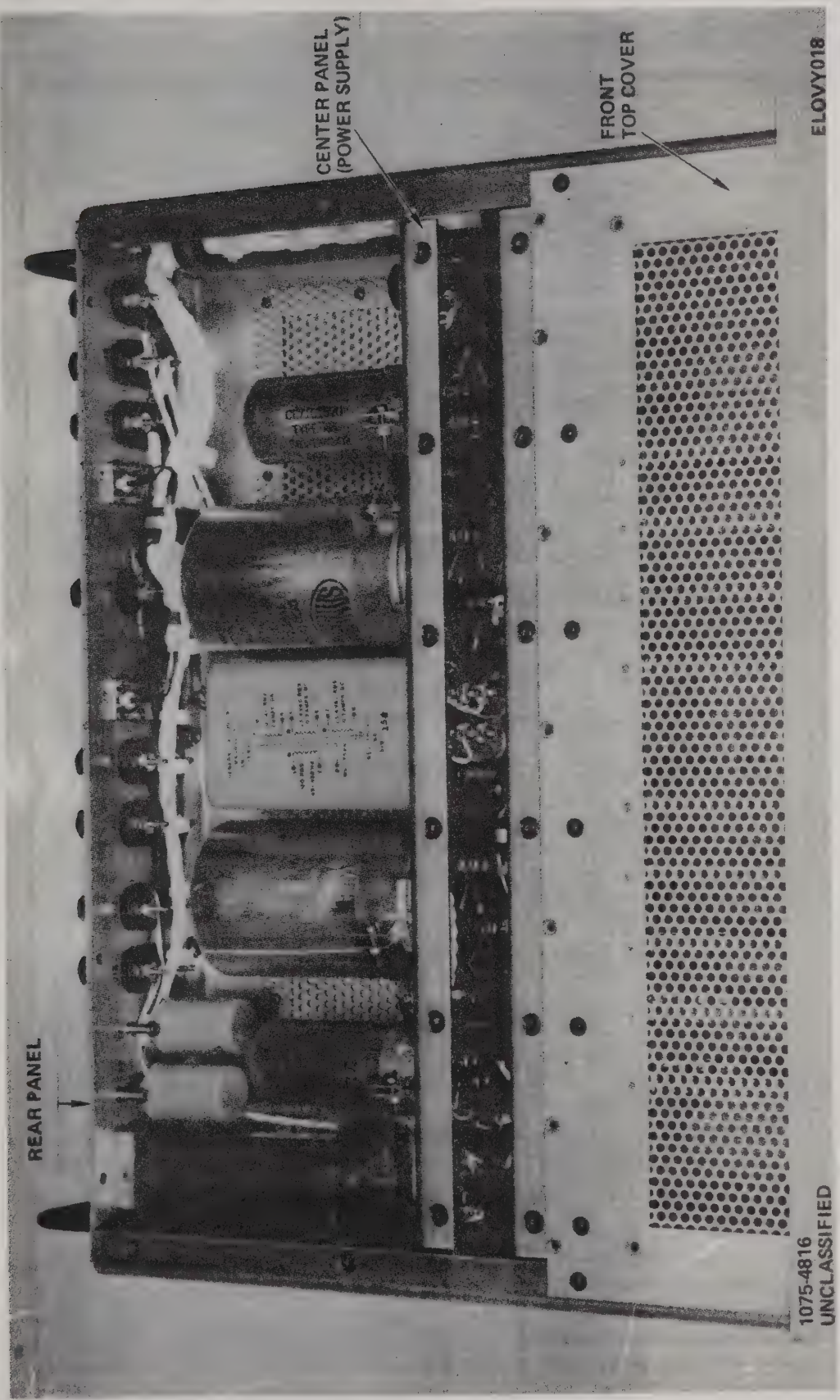


Figure 7-1. Top view of converter showing center panel and power supply.

7-5. Removal and Repair

The converter (fig. 7-2) contains five printed wiring boards, 1A1 through 1A5, in the transmitter section and four printed wiring boards, 1A6 through 1A9, in the receiver section. The printed wiring boards are located on connector mounting boards 1A10 and 1A11 which are connected to the wiring harnesses (fig. FO-4). Remove the power source before performing the following tasks.

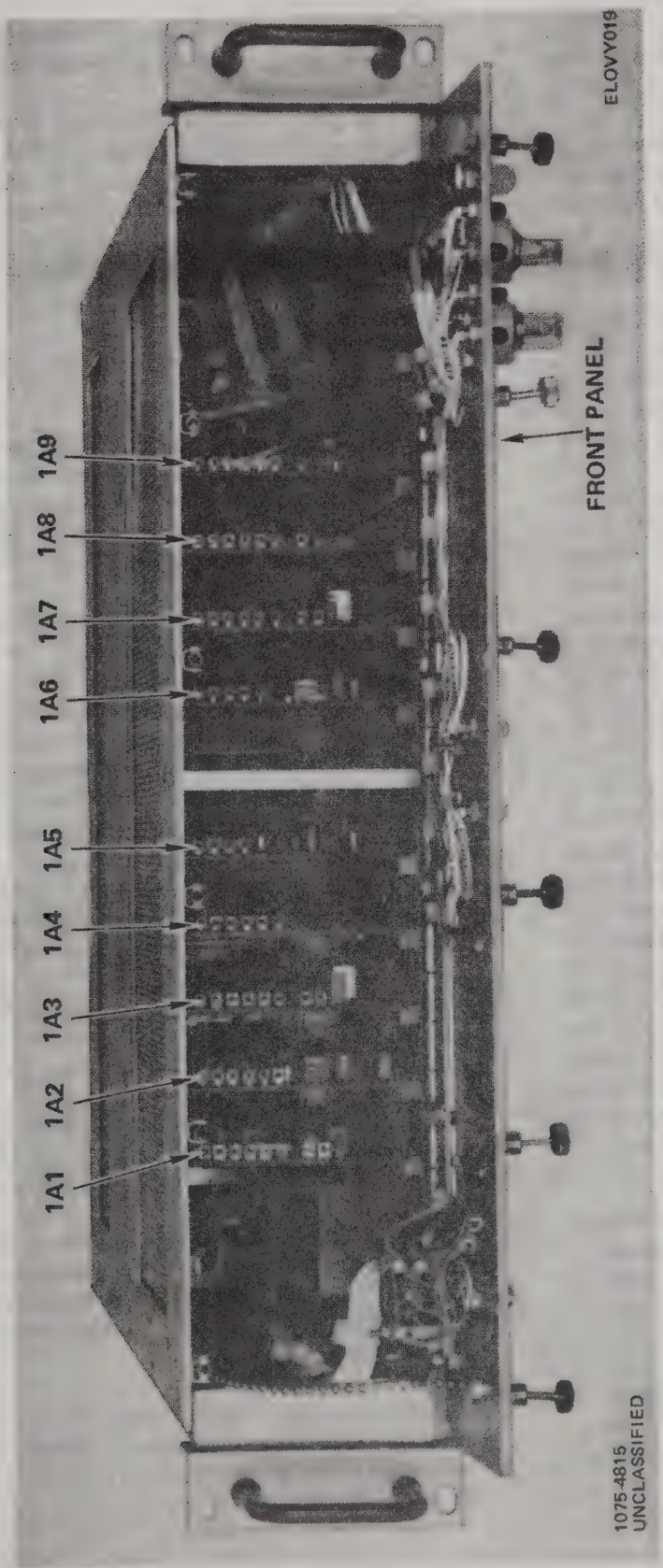


Figure 7-2. Front view of converter and location of printed wiring boards.

a. Removal of Converter From Rack. Remove converter from rack in reverse order of installation, refer to paragraphs 2-6 and 2-7.

b. General Parts Replacement. Observe the following when removing and replacing parts in the converter:

(1) A replacement part should be placed in the same position as that of the part removed and should be an exact duplicate. A replacement part that has the same electrical value as the original but differs in physical size may cause difficulty in reassembly.

(2) When replacing parts, use the same ground point as that used for the original wiring.

(3) Before unsoldering a part, note the position of the leads. If a part, such as a transformer, has many connections, tag each of the leads for ease in identification.

(4) Be careful when replacing diodes in the power circuit. Use a pencil soldering iron with a 25-watt maximum capacity. If the iron must be connected to an ac power source, use an isolating power transformer between the iron and the ac powerline.

(5) Solder diode leads quickly. Where wiring permits, use a heat sink (such as long-nose pliers) between the soldered joint and the diode. Use approximately the same length and dress of the original leads.

c. Harness Wiring Repair and Replacement. If wire insulation is broken or charred, or if the wire itself is broken, the method of replacement will be determined by the complexity of the cable harness and by the number of wires to be replaced. In a simple harness, repair the defective wires by removing the cable clamp and replacing the wire or wires. In a complex cable harness, repair by cutting the defective wires loose from the circuit at both ends and replacing them with good wires of the same gauge and length, then secure the new wires with the cable clamp. Be sure to remove all wire scraps and solder waste.

7-6. Disassembly

As a general rule, reverse the disassembly procedure to reassemble and replace converter components.

a. Replace Printed Wiring Board. Remove as follows:

CAUTION

Printed wiring boards should be removed (only with board extractor SMC 750009) and replaced carefully to avoid misalignment and damage to socket pins. When a board has been replaced, check for snug fitting in its respective socket.

(1) Place POWER switch to OFF position.

(2) Open front panel by loosening six captive mounting screws (fig. 7-2).

(3) Pull out printed wiring board using board extractor provided with equipment.

(4) During installation, note that boards are keyed properly to their respective sockets.

(5) Close front panel and tighten six captive screws.

(6) Place POWER switch on front panel to on position.

b. Replace Front Panel Parts. Disassemble parts from front panel as follows:

WARNING

120 vac is present at the rear panel power connector and line filter terminals, the front panel POWER switch and fuse terminals, and the power transformer on the center panel. Serious injury or DEATH may result from contact with these points.

(1) Disconnect power cable at power outlet.

(2) Open front panel by loosening six captive mounting screws (fig. 7-2).

(3) Unsolder leads and remove item (fig. 5-2).

(4) Assemble in reverse order of disassembly.

c. Replace Center Panel Parts. Remove power transformer T1, audio transformers T1 through T5, power supply filter capacitors C1 through C10, voltage regulators U1 through U4, and rectifier bridge diodes CR1 through CR12 as follows:

(1) Disconnect power cable at power outlet.

(2) Remove converter rear top cover (fig. 7-1).

CAUTION

Converter front top cover must be removed only at depot. Removing top front cover will require realignment of printed wiring board guides.

(3) Remove six screws attaching bottom flange of center panel to chassis and lift panel for access to parts (fig. 7-3).

CAUTION

Check polarity of all diodes before removal to be sure the correct polarity is maintained with the replacement. Incorrect polarity of supply voltage can result in serious damage to the unit.

NOTE

Before removing audio transformers T2 through T5, remove metal shield by twisting to break sealant.

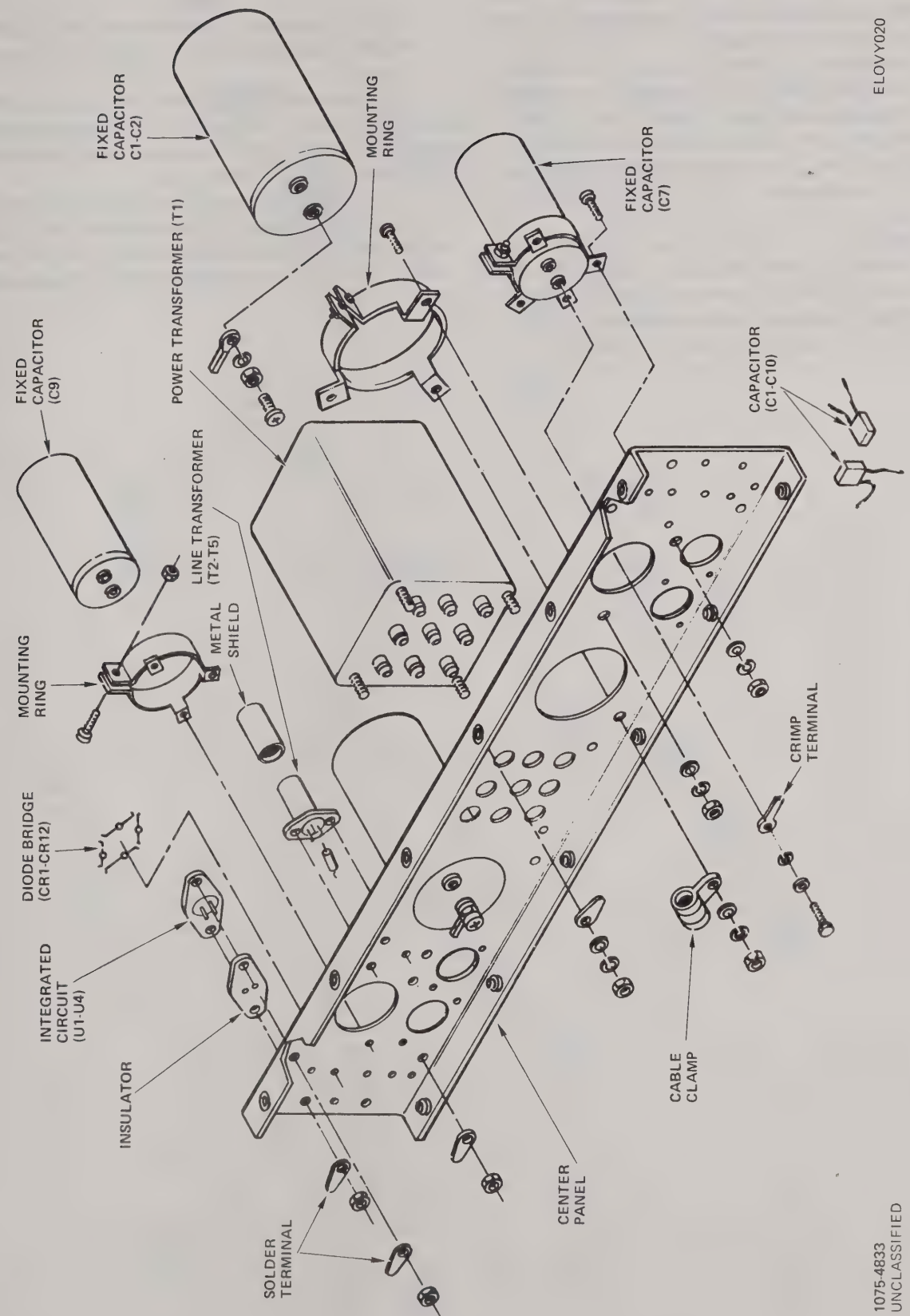


Figure 7-3. Center panel disassembly.

(4) Unsolder leads of item to be removed and disassemble from panel. Refer to paragraph 7-5*b* (4) and (5) for diode replacement.

(5) Assemble in reverse order of disassembly.

(6) After installing transformers T2 through T5, apply sealing compound (SM865138) to transformer case and secure metal shield to transformer.

d. Replace Rear Panel Parts. Remove powerline filter FL1, transformers T6 and T7, and connectors as follows:

(1) Perform *c*(1) and (2) above.

(2) Remove 12 mounting screws attaching rear panel and swing clear; be careful with cable harness.

(3) Remove connectors listed in table 7-6. Type of mechanical connection required is listed.

NOTE

Before removing transformers T6 or T7, remove metal shield by twisting to break sealant.

(4) Remove filter FL1 and transformers T6 and T7 (fig. 7-4) by removing attaching screws and unsoldering leads. The external power connector is an integral part of filter FL1.

(5) Assemble in reverse order of disassembly.

(6) After installing transformers T6 and T7, apply sealing compound (SMB865138) to transformer case and secure metal shield to transformer.

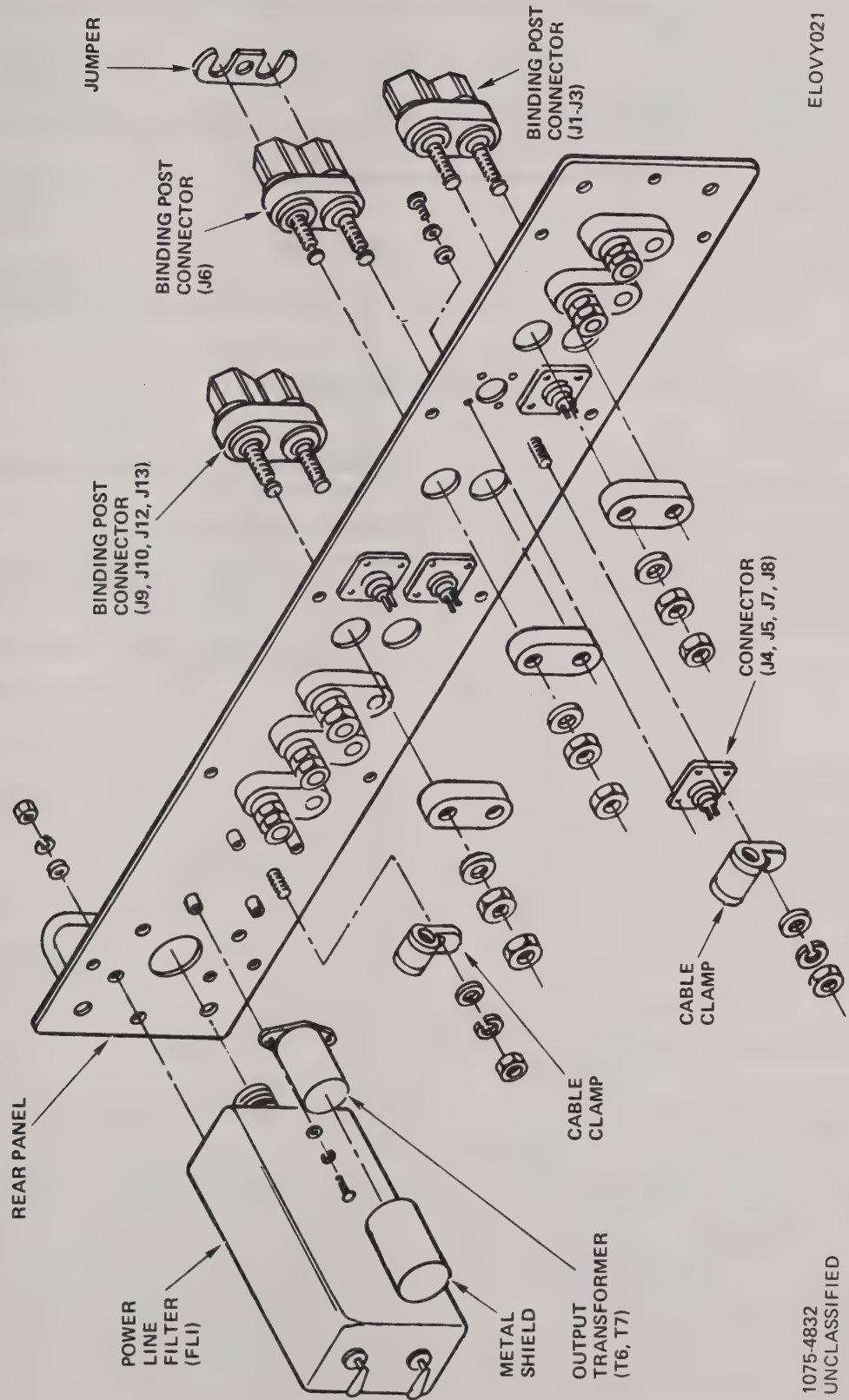


Figure 7-4. Rear panel disassembly.

Table 7-6. Rear Panel Connectors

Designation	Function	Type
J1	Transmitter input, low level voice	Binding post
J2	Transmitter input, high level voice	Binding post
J3	Transmitter input, hybrid	Binding post
J4, J5	Transmitter clock and data outputs, respectively	Twinaxial
J6	This pair of terminals provides for insertion of a fixed voltage between the circuit ground and the chassis ground. For 0 volt, a jumper connection is used.	Binding post
J7, J8	Receiver clock and data inputs, respectively	Twinaxial
J9	Receiver hybrid output	Binding post
J10	Receiver voice output	Binding post
J1	Power input	.....
J12	Transmitter output, 135 Ω	Binding post
J13	Receiver input, 135 Ω	Binding post

Section III. TESTING PROCEDURES

7-7. General

The locations of test jacks and variable resistors are shown in figure 5-3 and become accessible by opening the front panel. The common ground connection for the transmitter is test jack 1A1J9, and for the receiver, test jack 1A6J5. These are circuit ground connections, not necessarily chassis ground. Test equipment connections are made at the rear panel of the converter.

7-8. Checkout and Adjustment

For checkout and adjustment of the converter after repair or after shipment, perform the procedures given below.

a. Receiver Timing (Clock) Check (fig. 7-5). Perform check as follows:

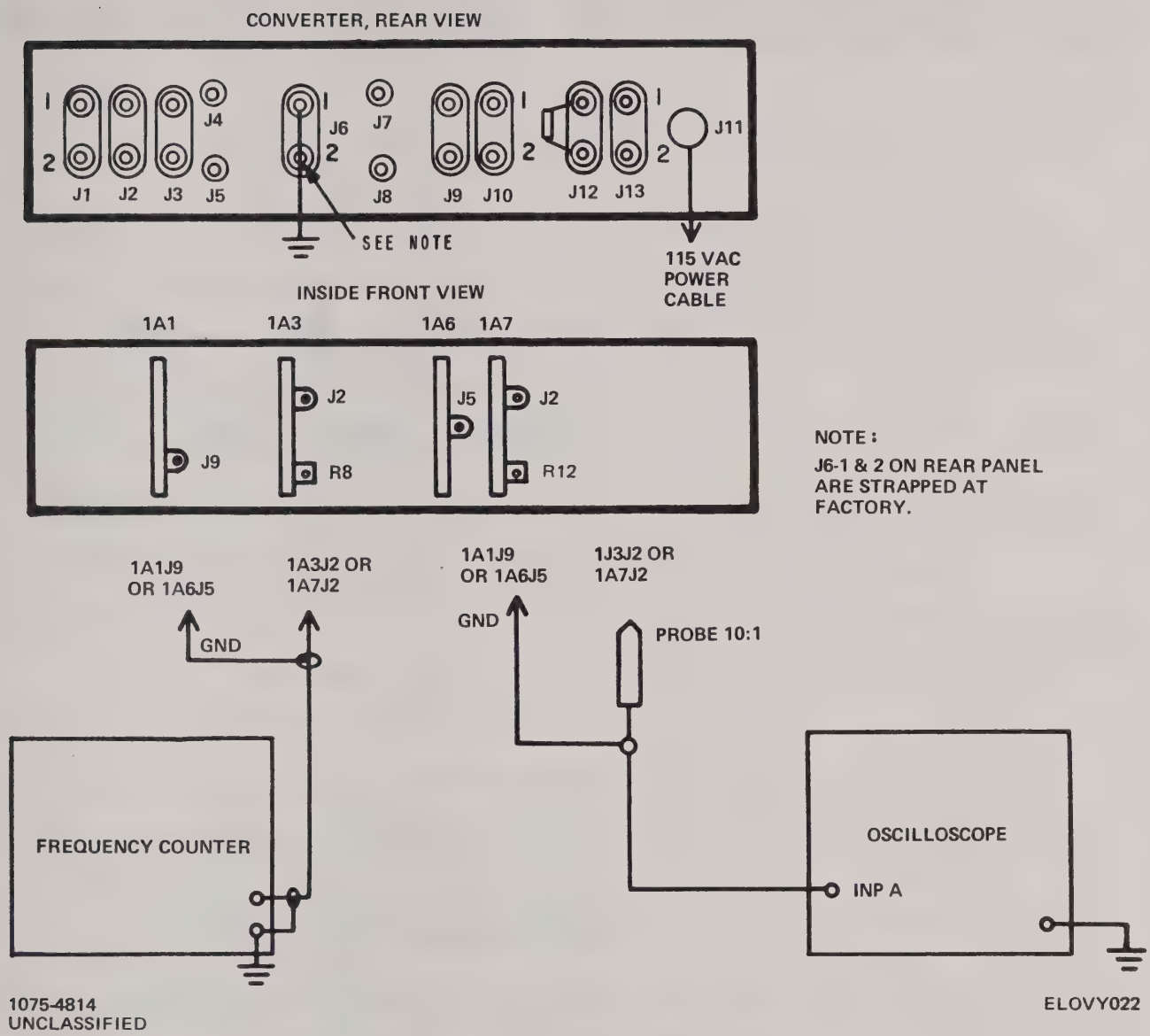


Figure 7-5. Receiver/transmitter timing (clock) check test setup.

NOTE

Clock frequency is critical for proper operation of the receiver. Be sure that the frequency counter used is correctly calibrated and warmed up.

(1) Check to see that there are no connections to rear panel jacks RCVR INPUT CLOCK J7, RCVR INPUT DATA J8, and RCVR INPUT (135 Ω) J13 to ensure that internal clock is free-running. See figure 2-3 for rear panel nomenclature.

(2) Check to see that receiver timing is strapped for external clock with terminals E1 and E2 of printed wiring board 1A7 (fig. 2-5) strapped together.

(3) Place POWER switch to ON position.

(4) Open front panel and connect frequency counter between 1A7J2 (fig. 5-3) and receiver ground jack 1A6J5.

(5) If frequency is not 7,200,000 ± 200 Hz, adjust variable resistor 1A7R12 to obtain correct value.

(6) If correct frequency cannot be obtained, remove printed wiring board 1A7 and replace with a board known to be good. Perform (5) above to recheck frequency.

(7) Remove frequency counter.

(8) Connect oscilloscope between test jack 1AJ2 and receiver ground 1A6J5; use a 10:1 probe. Adjust oscilloscope controls as shown in table 7-7 (waveform 1).

(9) Verify that waveform is as shown in table 7-7 (waveform 1).

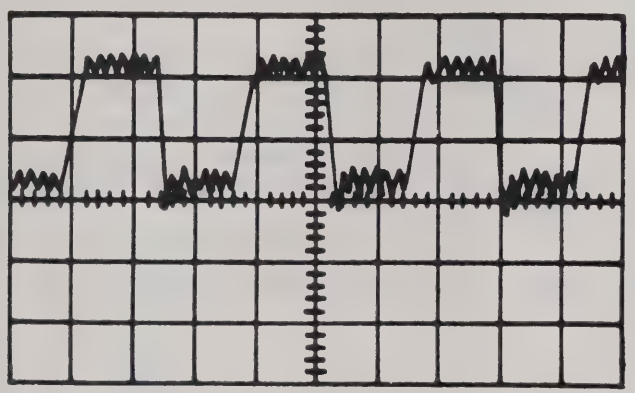
(10) If incorrect waveform is obtained, remove printed wiring board 1A7 and replace with a board known to be good. Recheck waveform.

(11) Remove oscilloscope, close front panel, tighten captive screws, and place POWER switch to OFF.

Table 7-7. Receiver/Transmitter Test Output Waveforms

WAVEFORM 1

Signal at Test Jacks 1A3J2 and 1A7J2



VERTICAL		HORIZONTAL	
SENS.	0.2V/DIV	SWEEP	0.05 μS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

UNIT SETUP

POSITION OF S2 HIGH LEVEL VOICE

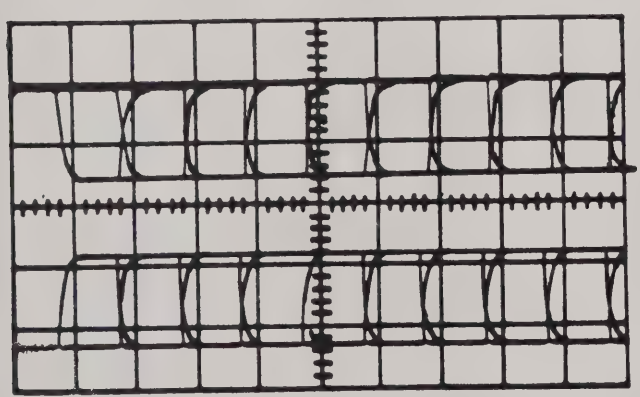
INPUT SIGNAL 1 kHz, 0 dBm

Note 1: Use 10:1 probe

Note 2: On oscilloscopes with limited bandwidth (5 MHz or 10 MHz) the signal appears as triangular waveform.

WAVEFORM 2

Signal at Test Jacks 1A5J3 and 1A5J4



VERTICAL		HORIZONTAL	
SENS.	2V/DIV	SWEEP	20 μS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	ALT	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

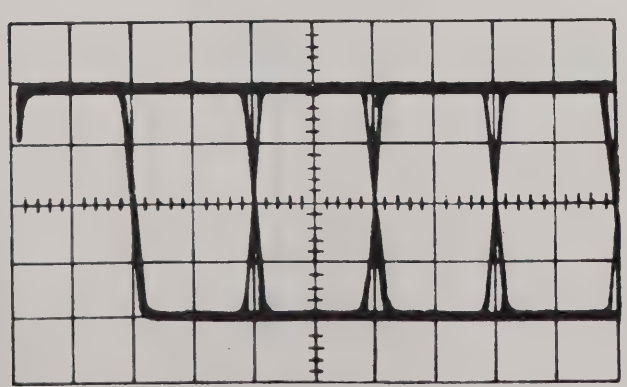
UNIT SETUP

POSITION OF S2 HIGH LEVEL VOICE

INPUT SIGNAL 1 kHz, 0 dBm

WAVEFORM 3

Signal at Rear Panel XMTR Output (135Ω)J12



VERTICAL		HORIZONTAL	
SENS.	0.2V/DIV	SWEEP	1.0 μS/DIV
COUPLING	DC	SYNC SOURCE	INT
MODE	CH1	SYNC FROM	
		SYNC MODE	NORM
		SLOPE	+
		COUPLING	LFREJ

UNIT SETUP

POSITION OF S2 HIGH LEVEL VOICE

INPUT SIGNAL 1 kHz, 0 dBm

b. Transmitter Timing (Clock) Check (fig. 7-5). Perform check as follows:

NOTE

Clock frequency is critical for proper operation of the transmitter. Be sure that the frequency counter is correctly calibrated and warmed up.

(1) Check to see that there is no connection to rear panel jack HYBRID XMTR INPUT J3 to insure that internal clock is free running.

(2) Set HIGH LEVEL VOICE/LOW LEVEL VOICE/HYBRID INPUT switch on front panel to either VOICE position.

(3) Place POWER switch on front panel to on position.

(4) Open front panel and connect frequency counter between test jack 1A3J2 and transmitter ground jack 1A1J9 (fig. 5-3).

(5) If frequency is not 7,200,000 ± 200 Hz, adjust variable resistor 1A3R8 to obtain correct value.

(6) If correct value cannot be obtained, remove printed wiring board 1A3 and replace with a board known to be good. Perform (5) above to recheck frequency.

(7) Remove frequency counter.

(8) Connect oscilloscope between test jack 1A3J2 and transmitter ground 1A1J9 use a 10:1 probe. Adjust oscilloscope controls as shown in table 7-7 (waveform 1).

(9) Verify that waveform is as shown in table 7-7 (waveform 1).

(10) If incorrect waveform is obtained, remove printed wiring board 1A3 and replace with a board known to be good. Recheck waveform.

(11) Remove oscilloscope, close front panel, tighten captive screws, and place POWER switch on front panel to OFF.

c. Transmitter Data Output (Bit Stream) Check (fig. 7-6). Perform check as follows:

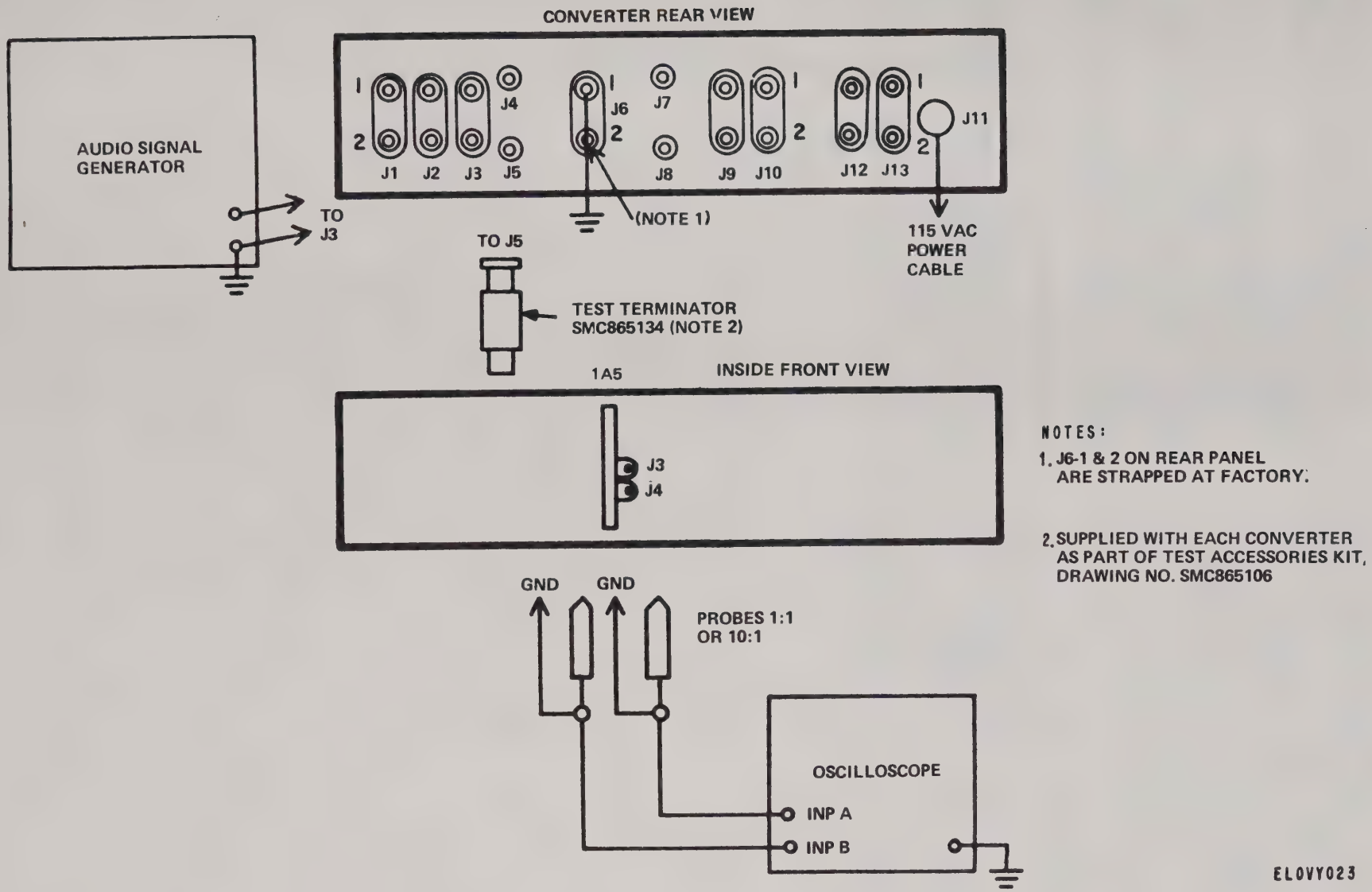


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Figure 7-6. Transmitter data output (bit stream) check test setup.

(1) Place a 75-ohm termination (table 7-1) at DATA XMTR OUTPUT jack J5 on rear panel. Connect a 130-ohm resistor (table 7-1) to terminals 1 and 2 of XMTR OUTPUT (135 Ω) J12 on rear panel. Connect J12 terminal 2 to ground.

(2) Connect audio signal generator to the HYBRID XMTR INPUT J3 on rear panel.

(3) Set audio signal generator for an output of 1 kHz at 1.0 ± 0.1 volts peak to peak using input B of oscilloscope for adjustment of level.

(4) Set HIGH LEVEL VOICE/LOW LEVEL VOICE/HYBRID INPUT switch on front panel to HYBRID INPUT.

(5) Place POWER switch to ON.

(6) Open front panel and connect oscilloscope input A to test jack 1A5J3 and input B to 1A5J4, using 1:1 or 10:1 probes. Adjust oscilloscope controls as shown in table 7-7 (waveform 2).

(7) Verify that waveform is as shown in table 7-7 (waveform 2).

(8) If incorrect waveform is obtained, remove printed wiring board 1A5 and replace with a board known to be good. Recheck waveform.

(9) Connect oscilloscope input A to XMTR OUTPUT (135 Ω) J12, terminal 1, on rear panel. Adjust oscilloscope controls as shown in table 7-7 (waveform 3).

(10) Verify that waveform is as shown in table 7-7 (waveform 3).

(11) If incorrect, replace printed wiring board 1A5. Recheck waveform, if still incorrect, refer to table 7-4.

(12) Remove all test equipment, close front panel, tighten captive screws, and place POWER switch to OFF.

7-9. Overall Converter Checks

A general check of converter operation can be made by using the transmitter output connected to receiver input to check individually both VOICE and DATA throughput as follows:

a. Voice Throughput Check (fig. 7-7). Perform check as follows:

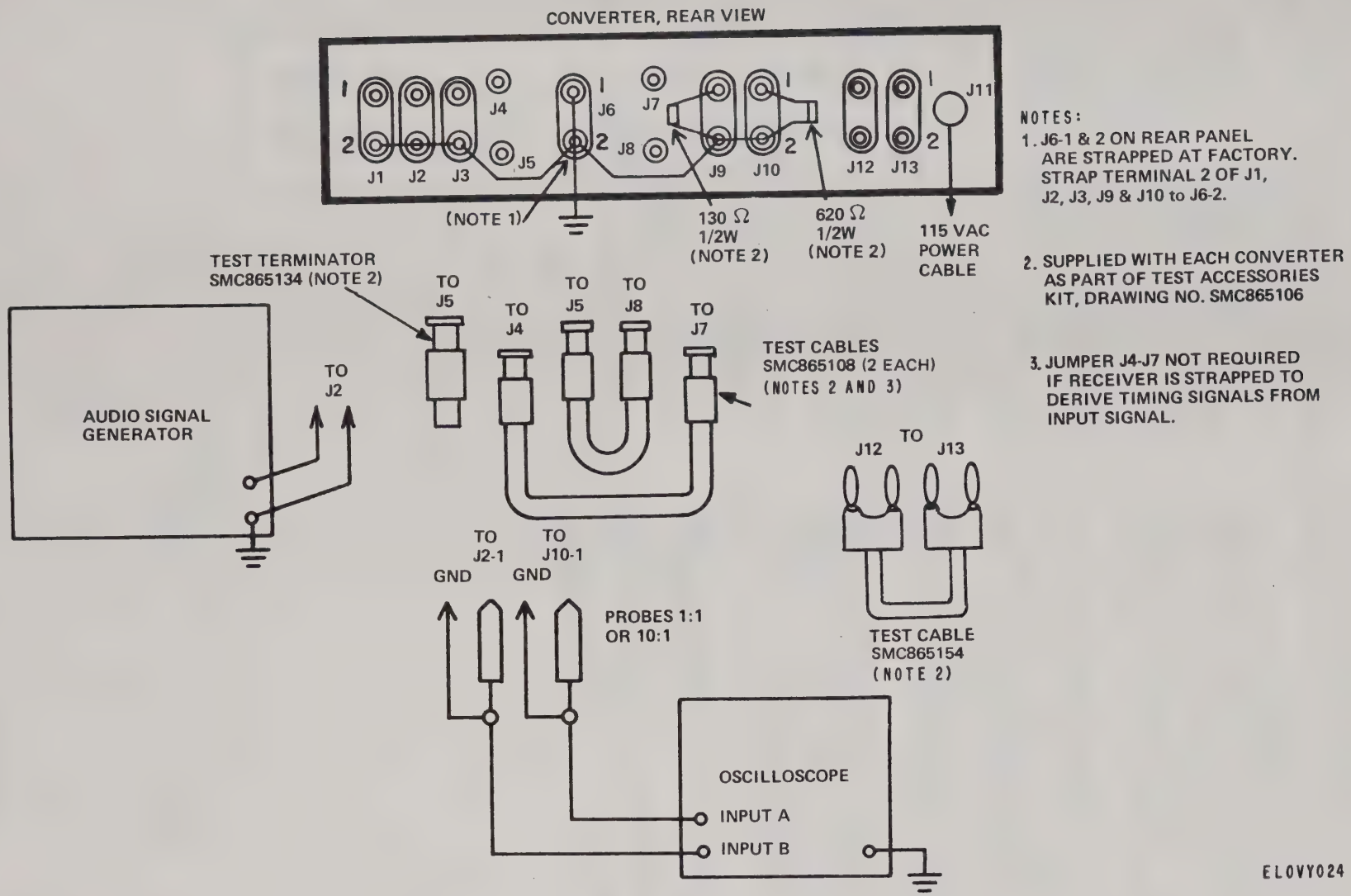

Figure 7-7. Voice throughput check test setup.

(1) Place POWER switch to OFF.

(2) Connect a test cable SMD865108 (table 7-1) between DATA XMTR OUTPUT J5 and DATA RCVR INPUT J8 on rear panel.

(3) If receiver is strapped for use with an external clock (para 2-10*d*), connect the second jumper cable SMD865108 between CLOCK XMTR OUTPUT J4 and CLOCK RCVR INPUT J7 on rear panel. A second cable is not required if the receiver is strapped to derive timing signals from input signals (para 2-7*c*).

(4) Connect a 620-ohm resistor (table 7-1) to terminals 1 and 2 of VOICE RCVR OUTPUT J10 on rear panel. Connect J10 terminal 2 to ground.

(5) Connect audio signal generator to HIGH LEVEL XMTR INPUT J2 on rear panel.

(6) Set HIGH LEVEL VOICE/LOW LEVEL VOICE/HYBRID INPUT switch on front panel to HIGH LEVEL VOICE.

(7) Connect input A of oscilloscope to VOICE RCVR OUTPUT J10 on rear panel, and input B to audio signal generator which is connected to HIGH LEVEL XTMR INPUT J2 on rear panel. Adjust oscilloscope controls as shown below:

Sensitivity IV/DIV with 1:1 probe	Sweep 0.2 m S/DIV
Coupling DC	Sync source INT
	Sync From
	Sync mode NORM
Mode ALT	Slope
	Coupling HF REJ

(8) Place POWER switch to ON.

(9) Check to see that both XMTR VOICE and RCVR VOICE indicator lamps are lighted.

(10) Set audio signal generator to 1 KHz at 2.5 $\pm$ 0.25 volts peak to peak.

(11) Observe waveform at VOICE RCVR OUTPUT J10 on rear panel. It is similar to audio signal generator output at HIGH LEVEL XMTR INPUT J2. With the strapping (E1 to E2) on printed wiring board 1A9 for low level output (para 2-7*b* and 2-10*c*), signal at VOICE RECEIVER OUTPUT J10 should be of equal amplitude to input signal at J2. It should be 2.5 $\pm$ 0.25 volts peak to peak. The output signal is factory set to the required level by variable resistor R15, and can be adjusted if required.

(12) To test the 135-ohm interface, perform (1) above, remove connections established in (2) above, and connect jumper cable SMC865154 with banana jacks (table 7-1) between XMTR OUTPUT (135) J12 and RCVR INPUT (135) J13. Connect 75-ohm terminator SMC865134 (table 7-1) to DATA XMTR OUTPUT J5.

NOTE

The polarity of the jumper cable is important, be sure banana jacks are inserted the same way, both with polarity indicator down.

(13) Repeat (3) through (11) above.

(14) Remove all test equipment.

b. Data Throughput Check (fig. 7-8). Perform check as follows:

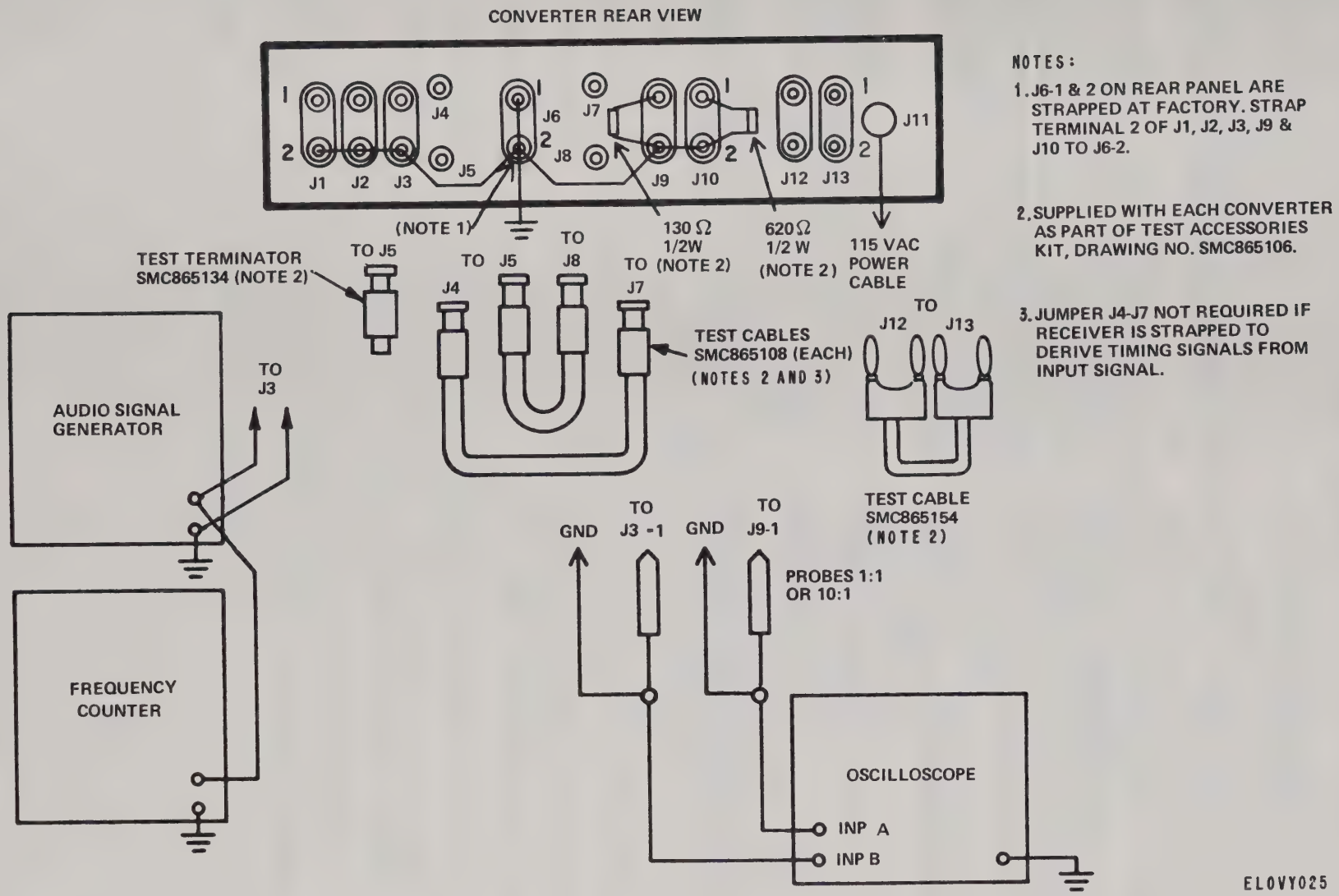

Figure 7-8. Data throughput check test setup.

(1) Place POWER switch to OFF and connect equipment as directed in *a*(2) and (3) above and as shown in figure 7-8.

(2) Connect a 130-ohm resistor (table 7-1) to terminals 1 and 2 of HYBRID RCVR OUTPUT J9 on rear panel. Connect J9 terminal 2 to ground.

(3) Connect audio signal generator to HYBRID XMTR INPUT J3 on rear panel.

(4) Set HIGH LEVEL VOICE/LOW LEVEL VOICE/HYBRID INPUT switch to HYBRID INPUT.

(5) Connect input A of oscilloscope to HYBRID RCVR OUTPUT J9 on rear panel, and input B to audio signal generator which is connected to HYBRID XMTR INPUT J3 on rear panel. Adjust oscilloscope controls as shown below:

Sensitivity 0.5V/DIV with 1:1 probe	Sweep 20mμS/DIV
Coupling DC	Sync source INT
	Sync from _____
	Sync mode NORM
Mode ALT	Slope _____
	Coupling HF REJ

(6) Place POWER switch to on position.

(7) Set audio signal generator to 25 kHz ±10Hz at 1.0±0.1 volt peak to peak using input B of oscilloscope for adjustment of level.

(8) Check to see that both XMTR DATA and RCVR DATA indicator lamps are lighted.

(9) Observe waveform at HYBRID RCVR OUTPUT J9, terminal 1. It should be a 25 kHz squarewave signal with relatively slow rise- and fall-times (50 Kbps consisting of alternating 1's and 0's), having a peak-to-peak amplitude of 0.8 ± 0.08 volt. This output is not adjustable; if incorrect, refer to table 7-4.

(10) Place POWER switch to OFF.

(11) Disconnect test cable SMD865108 (table 7-1) from between DATA XMTR OUTPUT J5 and DATA RCVR INPUT J8 on rear panel.

(12) To test the 135-ohm interface, connect jumper cable SMC865154 with banana jacks (table 7-1) between XMTR OUTPUT (135Ω) J12 and RCVR INPUT (135Ω) J13. Connect 75-ohm terminator SMC865134 (table 7-1) to DATA XMTR OUTPUT J5.

NOTE

The polarity of the jumper cable is important, be sure banana jacks are inserted the same way, both with polarity indicator down.

(13) Repeat (2) through (9) above.

(14) Remove all test equipment, close front panel, tighten captive screws, and place POWER switch to OFF.

APPENDIX A

REFERENCES

Following is a list of applicable references available to personnel concerned with Analog-Digital Converter CV-3034A/G:

DA Pam 310-4	Index of Technical Manuals, Technical Bulletins, Supply Manuals (Types 7, 8, and 9), Supply Bulletins, and Lubrication Orders.
DA PAM 310-7	US Army Equipment Index of Modification Work Orders.
SB 38-100	Preservation, Packaging, and Packing Materials, Supplies and Equipment Used by the Army.
SB 700-20	Army Adopted Items of Materiel and List of Reportable Items.
SC 5180-91-CL-R07	Tool Kit, Electronic Equipment TK-105/G.
TB 43-0118	Field Instructions for Painting and Preserving Electronics Command Equipment Including Camouflage Pattern Painting of Electrical Equipment Shelters.
TM 43-0139	Painting Instuctions for Field Use.
TM 11-6625-475-10	Operator's Manual: Multimeters AN/PSM-6, AN/PSM-6A, and AN/PSM 6B.
TM 11-5895-797-24P	Operator's, Organizational, Direct Support and General Support Maintenance Repair Parts (Including Depot Maintenance Repair Parts and Special Tools) for Analog-Digital Converter CV-3034A/G.
TM 11-6625-475-25	Organizational, DS, GS, and Depot Maintenance Manual: Multimeters AN/PSM-6, AN/PSM-6A, and AN/PSM-6B.
TM 11-6625-1537-15	Organizational, DS, GS, and Depot Maintenance Manual: Wide Range Oscillator Hewlett-Packard Model CD/CDR.
TM 11-6625-1541-15	Operator, Organizational, DS, GS, and Depot Maintenance Manual: Hewlett-Packard RMS Voltmeter Model 3400A.
TM 11-6625-1548-15	Organizational, DS, GS, and Depot Maintenance Manual: Counter, Electronic, Digital CP-772/U Hewlett-Packard Model 5245L.
TM 11-6625-1589-15	Organizational, DS, GS, and Depot Maintenance Manual: Hewlett-Packard Oscillator Model 204B.
TM 11-6625-1589-15-1	Operator's Organizational, DS, GS, and Depot Maintenance Manual:Hewlett-Packard Oscillator Model 204C.
TM 11-6625-1722-15	Operator's Organizational, Direct Support, General Support, and Depot Maintenance Manual Including Repair Parts and Special Tools Lists: Oscilloscope AN/USM-273.
TM 38-750	The Army Maintenance Management Systems (TAMMS).
TM 740-90-1	Administrative Storage of Equipment.
TM 750-244-2	Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).
TT-C-595	Colors, Federal Specification.

APPENDIX C

MAINTENANCE ALLOCATION

Section I. INTRODUCTION

C-1. General

This appendix provides a summary of the maintenance operations for CV-3034A/G. It authorizes categories of maintenance for specific maintenance functions on reparable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

C-2. Maintenance Function

Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i.e., to clean, preserve, drain, paint, or to replenish fuel/lubricants/hydraulic fluids or compressed air supplies.

d. Adjust. Maintain within prescribed limits by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipment used in precision measurement. Consists of the comparison of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment/system.

h. Replace. The act of substituting a serviceable like-type part, subassembly, model (component or assembly) for an unserviceable counterpart.

i. Repair. The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or resurfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module/component/assembly, end item or system. This function does not include the trial and error replacement of running spare type items such as fuses, lamps, or electron tubes.

j. Overhaul. That periodic maintenance effort (service/action) necessary to restore an item to a completely serviceable/operational condition as prescribed by maintenance standards (e.g., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like-new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like-new condition in accordance with original manufacturing standards. Rebuild is the highest degree of material maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipment/components.

C-3. Column Entires

a. Column 1, Group Number. Column 1 lists group numbers, the purpose of which is to identify components, assemblies, subassemblies and modules with the next higher assembly.

b. Column 2, Component/Assembly. Column 2 contains the noun names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

c. Column 3, Maintenance Function. Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide.

d. Column 4, Maintenance Category. Column 4 specifies, by the listing of a "worktime" figure in the

appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated category of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance categories, appropriate "worktime" figures will be shown for each category. The number of man-hours specified by the "worktime" figure represents the average time required to restore an item (assembly, subassembly, component, module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

C—Operator/Crew
O—Organizational
F—Direct Support
H—General Support
D—Depot

e. Column 5, Tools and Equipment. Column 5 specifies by code, those common tool sets (not individual tools) and special tools, test, and support equipment required to perform the designated function.

C-4. Tool and Test Equipment Requirements (Table 1)

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Category. The codes in this column indicate the maintenance category allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NATO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for Manufacturers (5-digit) in parentheses.

Next printed page is C-3).

SECTION II MAINTENANCE ALLOCATION CHART FOR

ANALOG-DIGITAL CONVERTER CV-3034A/G

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQUIPMENT
			C	O	F	H	D	
00	ANALOG-DIGITAL CONVERTER CV-3034A/G	Inspect[1]	0.1					
		Inspect[2]		0.3				
		Test[3]		0.5				2,18
		Test			1.0			3 thru 8, 18
		Service[4]		0.2				
		Adjust[5]			0.5			1,3
		Replace			0.2			
		Repair[7]		0.2				2,18
		Repair			1.0			1 thru 8, 18
		Overhaul					4.0	1 thru 19
01	CHASSIS, FRONT PANEL	Inspect[8]		0.1				
		Test[3]		0.5				2,18
		Repair[7]		0.2				2,18
		Repair			1.0			1 thru 8, 18
02	CHASSIS, CENTER PANEL	Inspect		0.2				
		Test[3]		0.5				2,18
		Repair			1.0			1 thru 8, 18
03	CHASSIS, REAR PANEL	Inspect[3]		0.3				
		Test[3]		0.5				2,18
		Repair			1.0			1 thru 8, 18
04	CONNECTOR MOUNTING ASSEMBLY 1A10	Test[9]			0.5			2,18
		Replace			1.0			2,18
		Repair					1.0	1 thru 19
05	CONNECTOR MOUNTING ASSEMBLY 1A11 (See group 04)							
06	TRANSMITTER FILTER BOARD 1A1	Test[10]			1.0			1 thru 8, 18
		Test					0.5	1 thru 19
		Replace			0.1			
		Repair					2.0	1 thru 19
07	TRANSMITTER ANALOG-TO-DIGITAL BOARD 1A2 (See group 06)							
08	TRANSMITTER TIMING BOARD 1A3 (See group 06)							
09	TRANSMITTER DATA PRESENCE BOARD 1A4 (See group 06)							
10	TRANSMITTER INTERFACE BOARD 1A5 (See group 06)							
11	RECEIVER DIGITAL-TO-ANALOG BOARD 1A6 (See group 06)							
12	RECEIVER TIMING BOARD 1A7 (See group 06)							
13	RECEIVER SEQUENCE DETECTOR BOARD 1A8 (See group 06)							
14	RECEIVER FILTER BOARD 1A9 (See group 06)							
15	LINE CORD ASSEMBLY W1	Test		0.1				2,18
		Repair		0.5				2,18
16	EXTENDER BOARD XA1 AND XA2	Inspect		0.1				2,18
		Test		0.1				2,18
		Repair		0.5				2,18

(1) Limited to visual inspection and wiping clean exterior surfaces.
(2) Limited to external visual inspection including checking cables for fraying or chafing, and input/output and power cable rear panel connections for firmness.
(3) Limited to performing power supply voltages check.
(4) Limited to replacement of fuse cartridges and power indicator lamp.
(5) Limited to adjustment made during performance of overall unit check.
(6) Not used.
(7) Limited to replacement of indicator lamps with soldered connections, lampholders and fuseholders.
(8) Limited to internal visual inspection.
(9) Limited to continuity checks only.
(10) Limited to fault isolation to printed wiring board.

TABLE 1. TOOL AND TEST EQUIPMENT REQUIREMENTS FOR

ANALOG-DIGITAL CONVERTER CV-3034A/G

TOOL OR TEST EQUIPMENT REF CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL/NATO STOCK NUMBER	TOOL NUMBER
1	F,H,D	FREQUENCY COUNTER CP-772/U	6625-00-922-3586	HP-5245L (28480)
2	O,F,H,D	MULTIMETER AN/PSM-6B or AN/USM-210	6625-00-019-0815	
3	F,H,D	OSCILLOSCOPE AN/USM-273	6625-00-930-6637	TEK-453 (80009)
4	F,H,D	TRUE RMS VOLTMETER AN/USM-224	6625-00-912-4434	HP-3400 (28480)
5	F,H,D	AUDIO SIGNAL GENERATOR SG-632/U or O-1025U (2 required)	6625-00-865-9026	HP-204B (28480)
6	F,H,D	TEST ACCESSORIES KIT*		SMB865106 (80063)
		TEST CABLES		SMD865108 and SMC865154 (80063)
		RESISTOR, 620 OHMS, 5%, 1/2W	5905-00-279-1761	RCR20G621J
		RESISTOR, 130 OHMS, 5%, 1/2W	5905-00-252-5436	RCR20G131J
		TERMINATOR, 75 OHMS		SMC-865134 (80063)
7	F,H,D	EXTENDER BOARD ASSEMBLY		SMD750075 (80063)
8	F,H,D	BOARD EXTRACTOR		SMC750009 (80063)
9	D	DISTORTION ANALYZER AN/USM-259		
10	D	FIA NOISE WEIGHTING FILTER		BP-FIA-8-10K-B (25844)
11	D	TEST SET #1 (for testing 1A1 and 1A9)		SMB879591 (80063)
12	D	TEST SET #2 (for testing 1A2)		SMB879592 (80063)
13	D	TEST SET #3 (for testing 1A3, 1A5, and 1A7)		SMB879593 (80063)
14	D	TEST SET #4 (for testing 1A4)		SMB879594 (80063)
15	D	TEST SET #5 (for testing 1A6)		SMB879595 (80063)
16	D	TEST SET #6 (for testing 1A8)		SMB879596 (80063)
17	D	MAINTENANCE KIT, ELECTRONIC EQUIPMENT MK-984/U or MK-772 where available	6625-00-930-1658 5999-00-757-7042	
18	O,F,H,D	TOOL KIT, ELECTRONIC EQUIPMENT TK-105/G	5180-00-610-8177	
19	D	TOOL KIT, ELECTRONIC EQUIPMENT TK-100/G	5180-00-605-0079	

*Supplied with CV-3034A/G

ANSEL-MA Form 1 OCT 74 6013

HISA-FM 2881-74

GLOSSARY OF ABBREVIATIONS AND SIGNAL MNEMONICS

	C
CIN	Clock Input Negative
CIP	Clock Input Positive
COM	Comparison
CON	Clock Output Negative
COP	Clock Output Positive
	D
DAO	Digital-to-Analog Output
DCON	Digital Clock Output Negative
DCOP	Digital Clock Output Positive
DDF	Digital Data Frequency
DDON	Digital Data Output Negative
DDOP	Digital Data Output Positive
DIN	Data Input Negative
DINA	Data Input Negative Alternate
DIP	Data Input Positive
DIPA	Data Input Positive Alternate
DON	Data Output Negative
DOP	Data Output Positive
DOPA	Data Output Positive Amplified
DSL	Digital Signal Level
DVS	Digitized Voice Sample
	E
EDGES	Edge Sync
EQ	Equal Inputs
	F
50KBVD	50 Kilobits Voice Data
	G
GASYN	Gated Synthetic
	H
HICCUP	Shifts the search for the random sequence to the next group of bits.
	I
ID	Incoming Data
	L
LSB	Least Significant Bit
LOAD	Loads or shifts signal into shift register to check for pseudorandom sequence
LPFOC	Low-Pass Filter Output Capacitively-Coupled
	M
MC	Mode Control
MSB	Most Significant Bit
	P
PT	Passed Threshold
	R
RD	Reclocked Data
RHO	Receiver Hybrid Output
ROM	Read Only Memory
RVO	Receiver Voice Output
	S
SEL DATA	Selected Data
	T
	Timing Signals (Receiver)—See Note paragraph 6-4
	Timing Signals (Transmitter)—See Note paragraph 6-3
	V
VORD	Voice or Data

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PUBLICATION NUMBER	DATE	TITLE
TM 11-5840-340-12	23 Jan 74	Radar Set AN/PPC-76

BE EXACT. . .PIN-POINT WHERE IT IS				IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
PAGE NO.	PARAGRAPH	FIGURE NO.	TABLE NO.	
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		F03		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. + 24 VDC is the input voltage.

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SSG I. M. DeSpiritof 999-1776	SSG I. M. DeSpiritof

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NG: None

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For explanation of abbreviations used, see AR 310-50.

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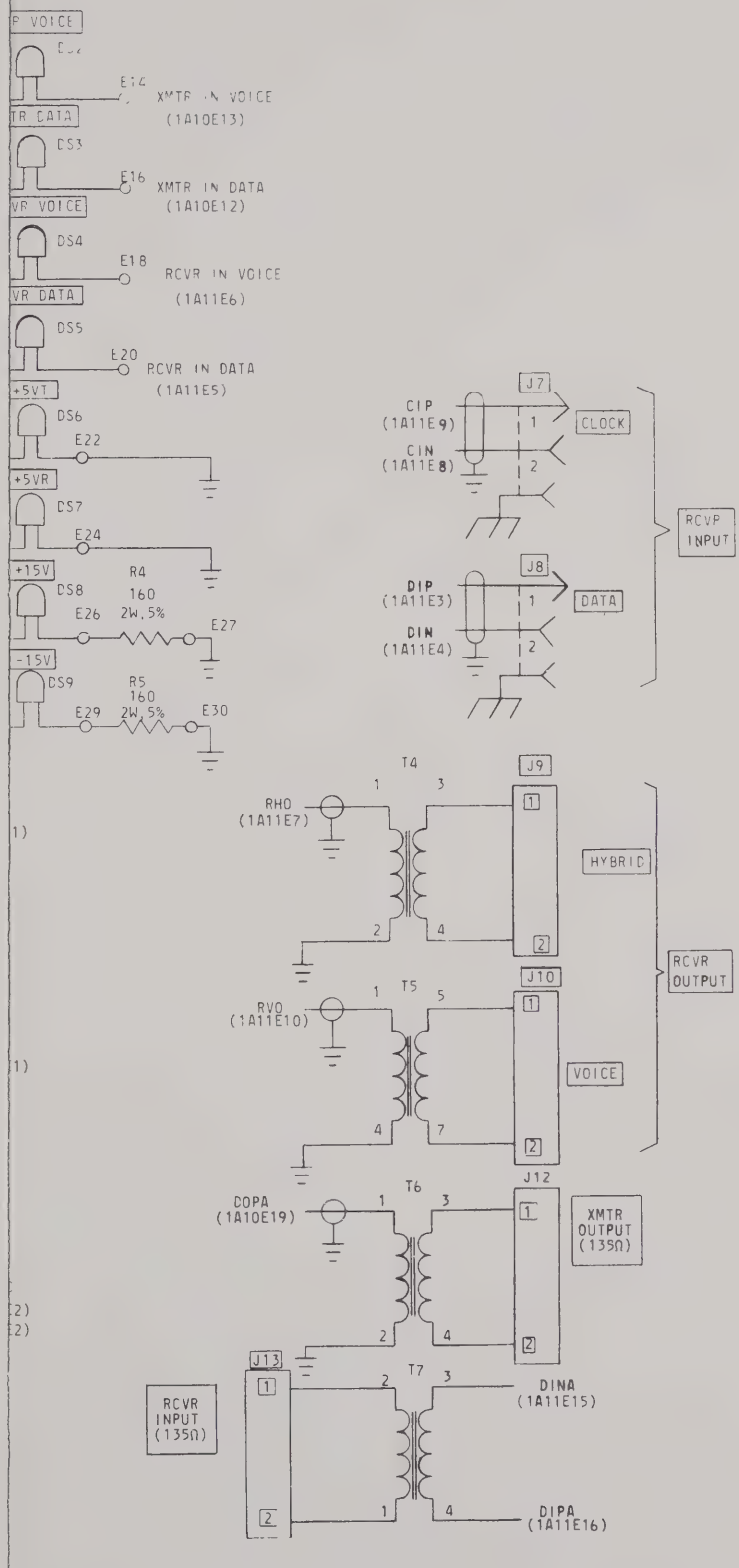


Chassis schematic diagram.

NOTES:

1. UNLESS OTHERWISE INDICATED, ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4 W. CAPACITOR VALUES ARE IN MICROFARADS.
2. ⇨ INDICATES CONNECTOR PIN OF P1.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1.

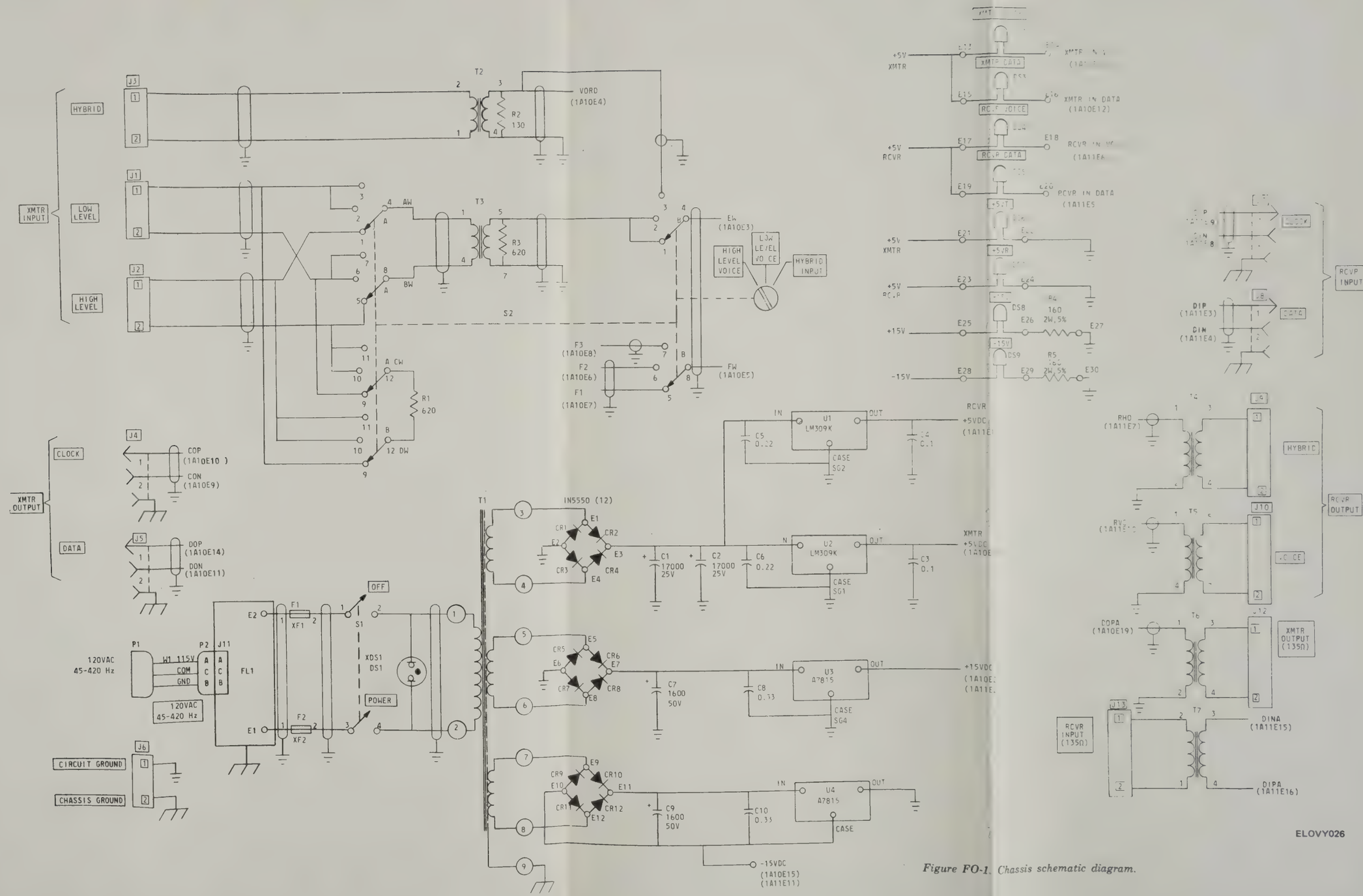
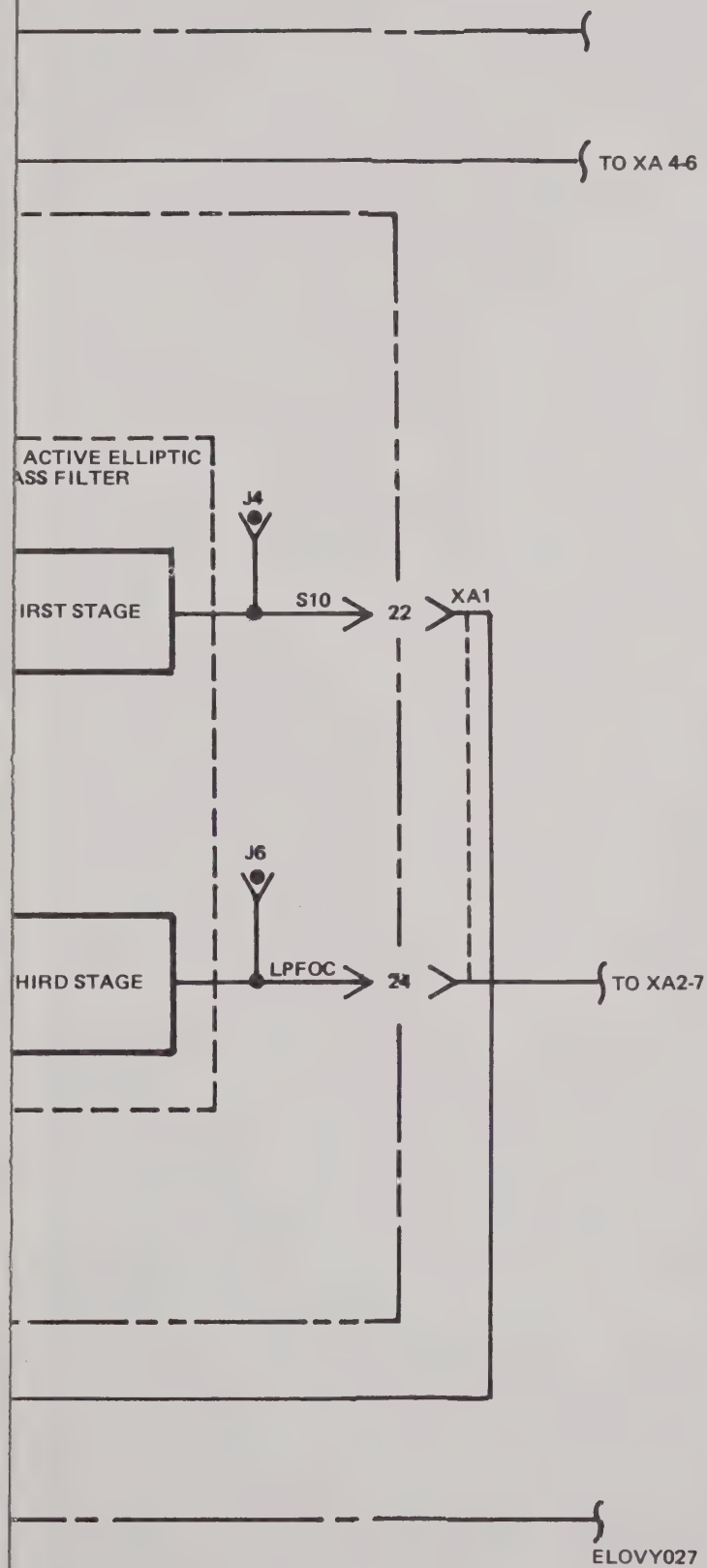


Figure FO-1. Chassis schematic diagram.



ter functional diagram (*sheet 1 of 3*).

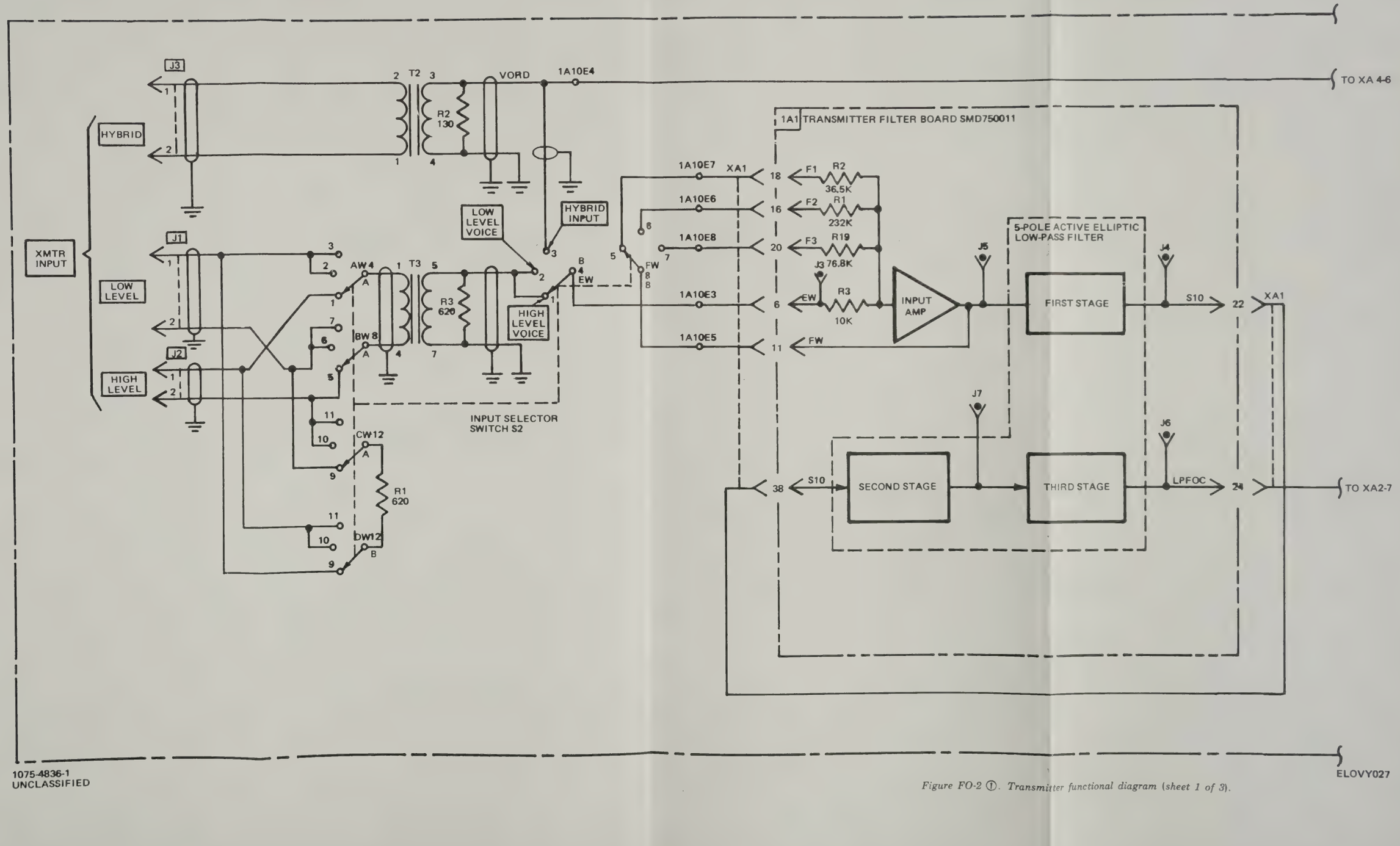
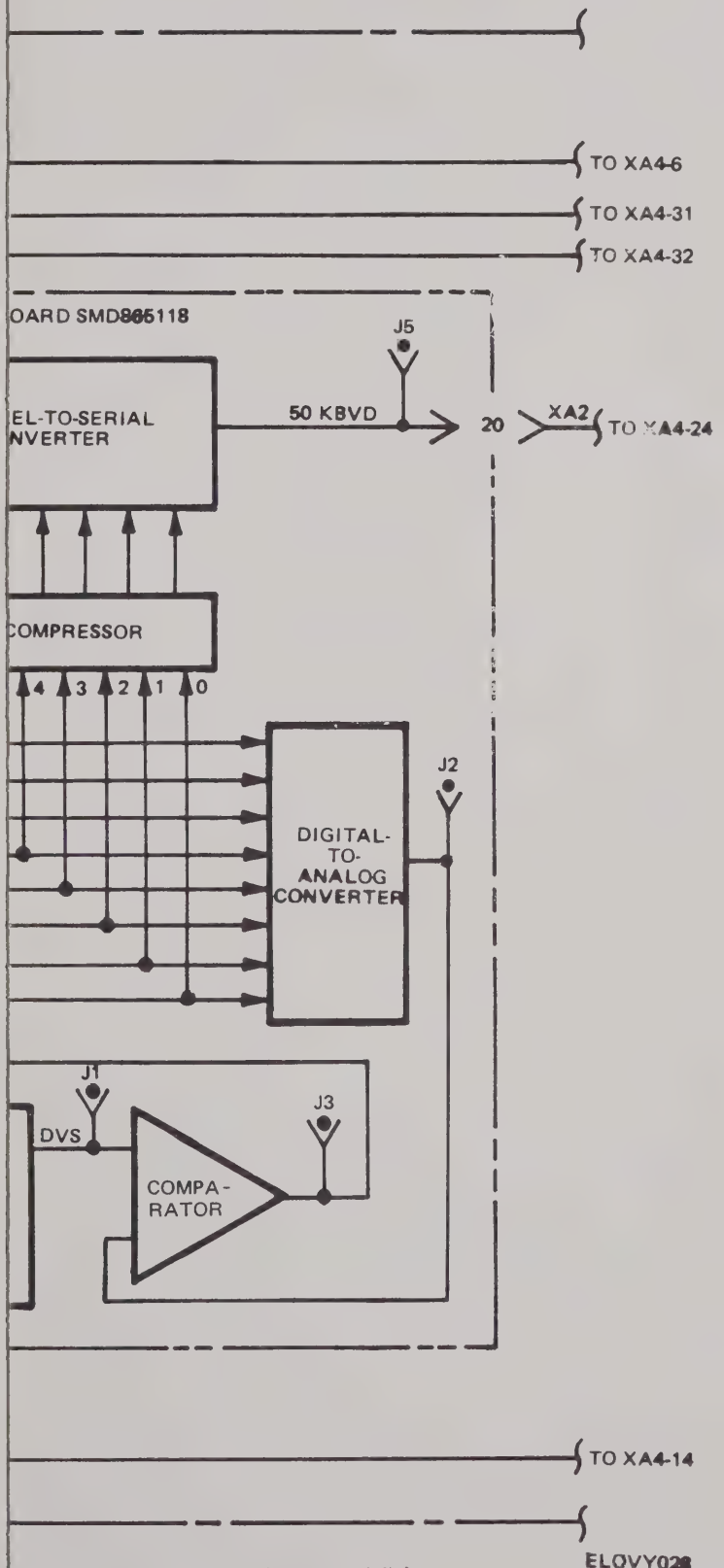


Figure FO-2 ①. Transmitter functional diagram (sheet 1 of 3).



nitter functional diagram (sheet 2 of 3).

TO XA10E4

TO XA4-6

TO XA4-31

TO XA4-32

1A3 TRANSMITTER TIMING BOARD SMD750013

7.2 MHz CRYSTAL OSCILLATOR

J2

DIVIDE-BY-2

3.6 MHz

DIVIDE-BY-9

400 kHz

BO

J6

XA3 27 GASYN

FREQUENCY CONTROLLER

C SCALER

J3

G SCALER

G0 8

$\overline{G0}$ 7

C2 12

C0 26

C1 24

XA3

C2

$\overline{D0}$

D3

K0

K1

SYNCHRO-NIZER

D SCALER

J5

K SCALER

K0 19

K1 14

D3 18

$\overline{D0}$ 23

D1 16

D2 15

D0 20

$\overline{D3}$ 22

J8

J4

J7

1A2 TRANSMITTER ANALOG-TO-DIGITAL BOARD SMD866118

XA2

23 G0

15 C2

14 $\overline{D0}$

12 D3

38 K0

24 K1

PARALLEL-TO-SERIAL CONVERTER

50 KBVD

J5

20 XA2 TO XA4-24

7-BIT PSEUDO-RANDOM SEQUENCE GENERATOR

SEQ

J4

ROM COMPRESSOR

MSB 7 6 5 4 3 2 1 0

11 C0

10 C1

8 D0

16 D1

18 D2

8-BIT STORAGE REGISTER

A0

A1

A2

0 LSB

$\overline{COM}$

DIGITAL-TO-ANALOG CONVERTER

J2

6 $\overline{D3}$

7 LPFOC

SAMPLE AND HOLD

J1

DVS

COMPA-RATOR

J3

TO XA1-24

TO XA4-14

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Figure FO-2 ②. Transmitter functional diagram (sheet 2 of 3).

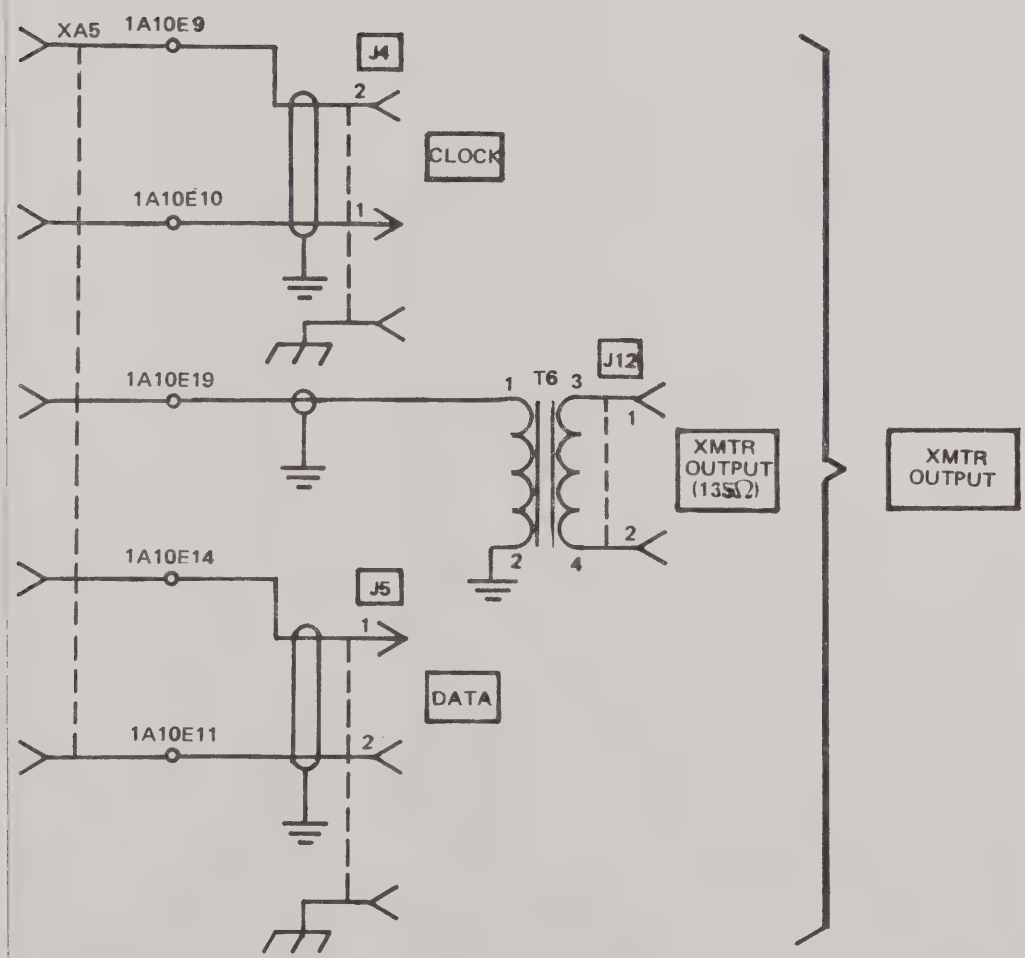

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Figure FO-2 ③. Transmitter functional diagram (sheet 3 of 3).

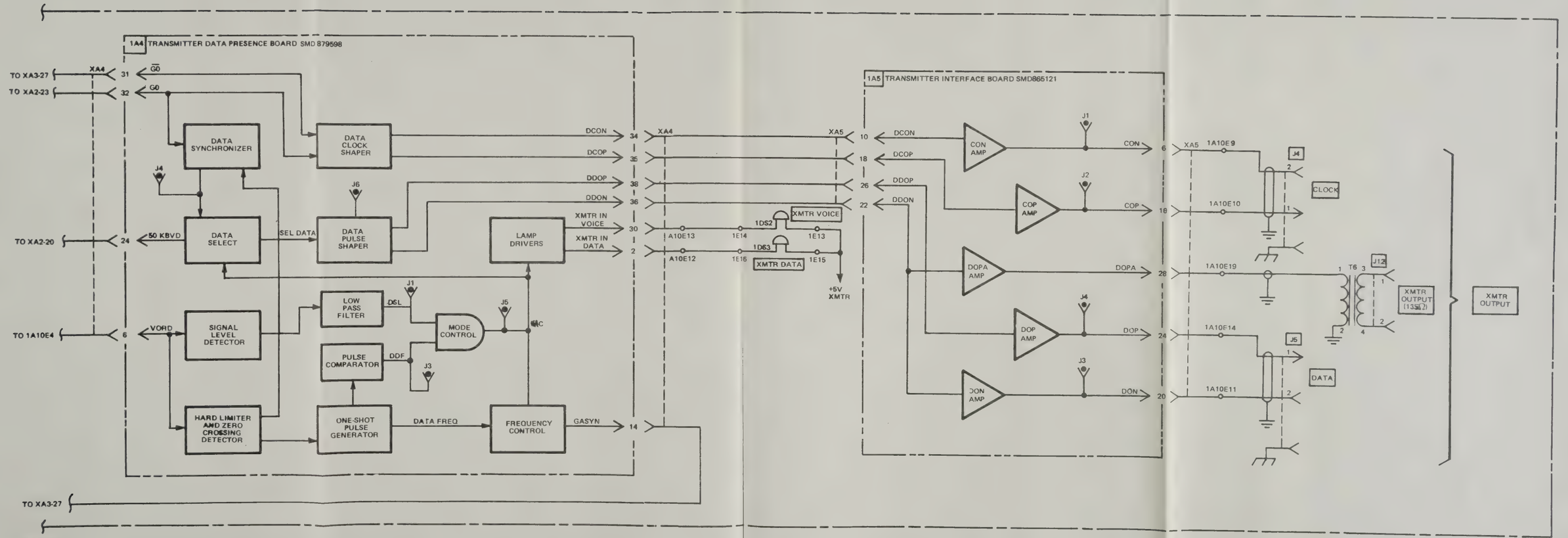

Figure FO-2 ③. Transmitter functional diagram (sheet 3 of 3).

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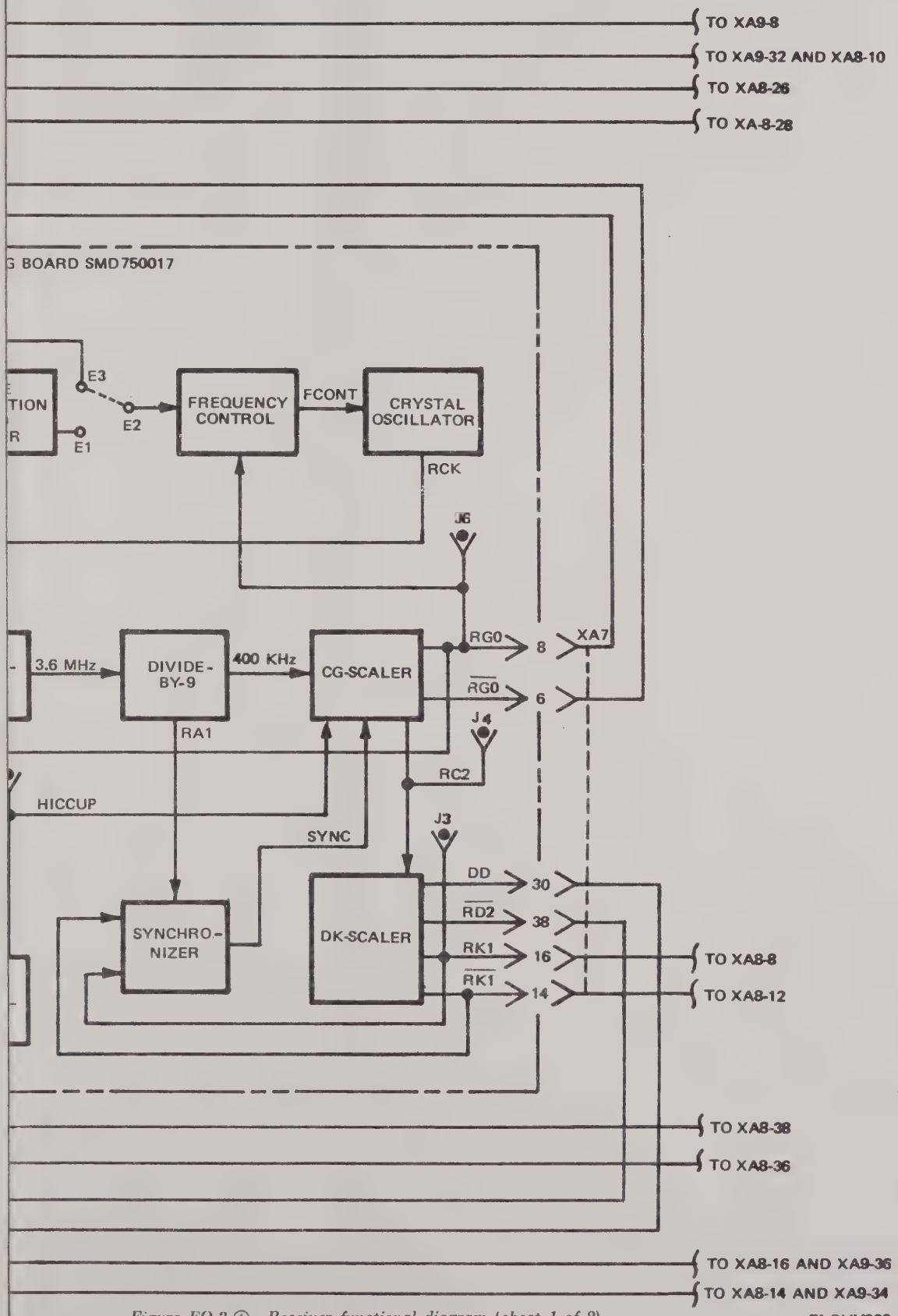

Figure FO-3 ①. Receiver functional diagram (sheet 1 of 2).

ELOVY030

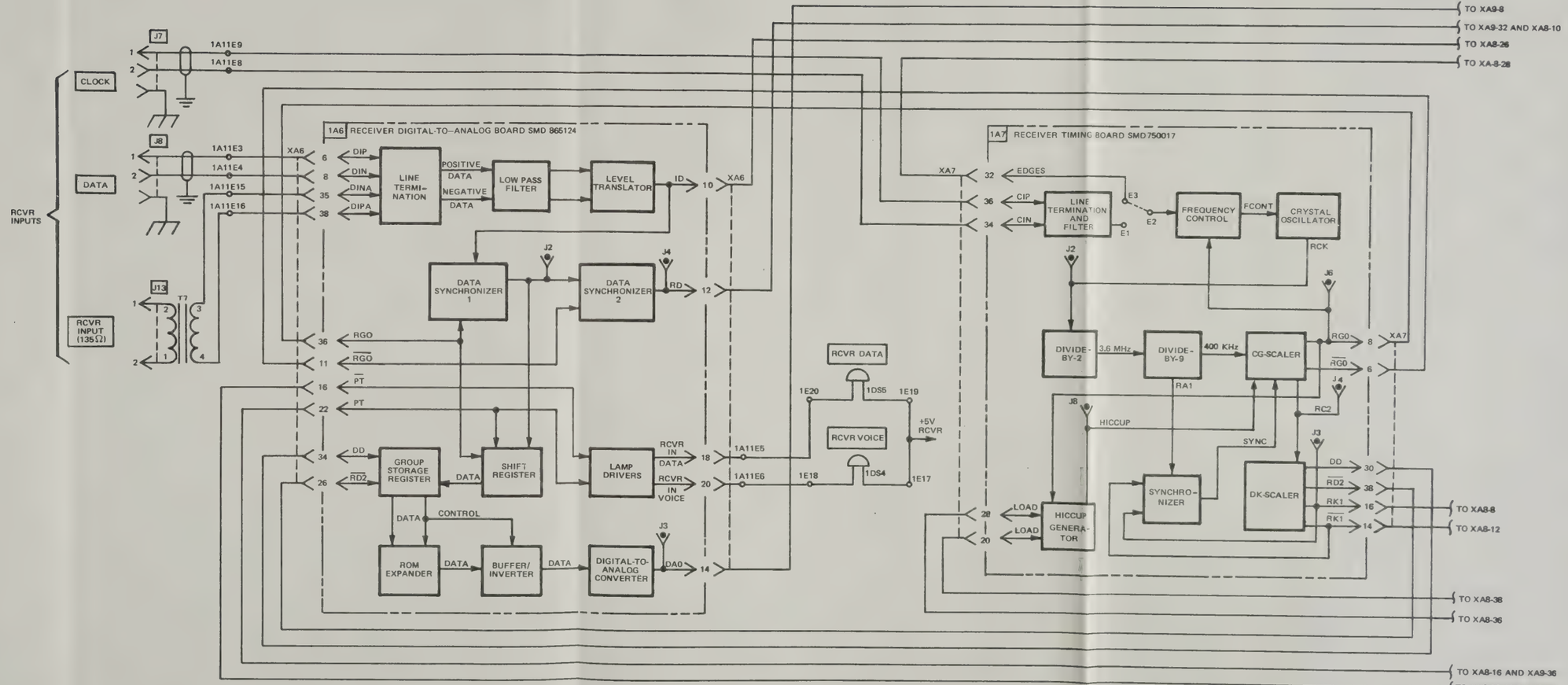

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Figure FO-3 ①. Receiver functional diagram (sheet 1 of 2).

ELOVY030

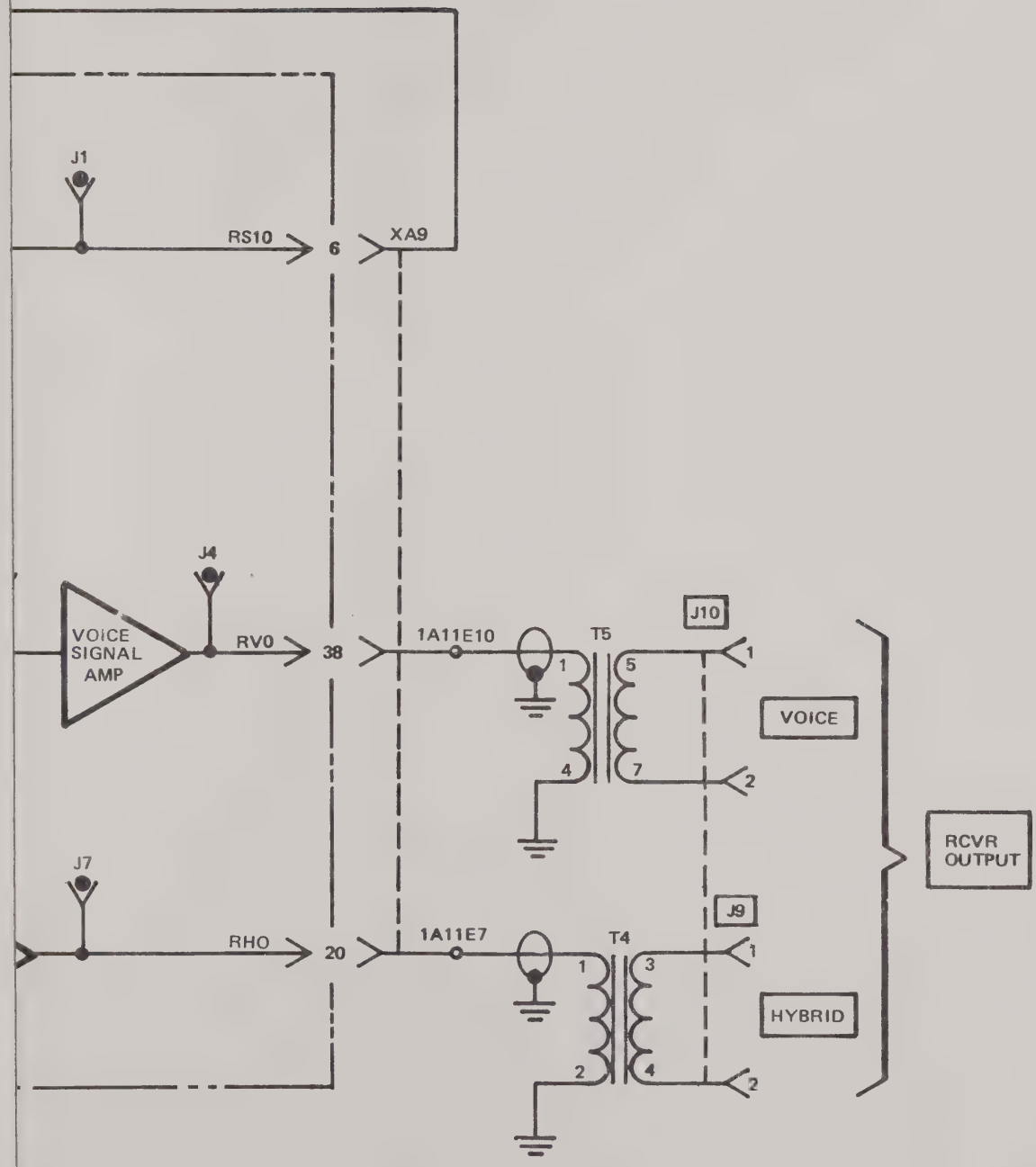


Figure FO-3 ②. Receiver functional diagram (sheet 2 of 2).

ELOVY031

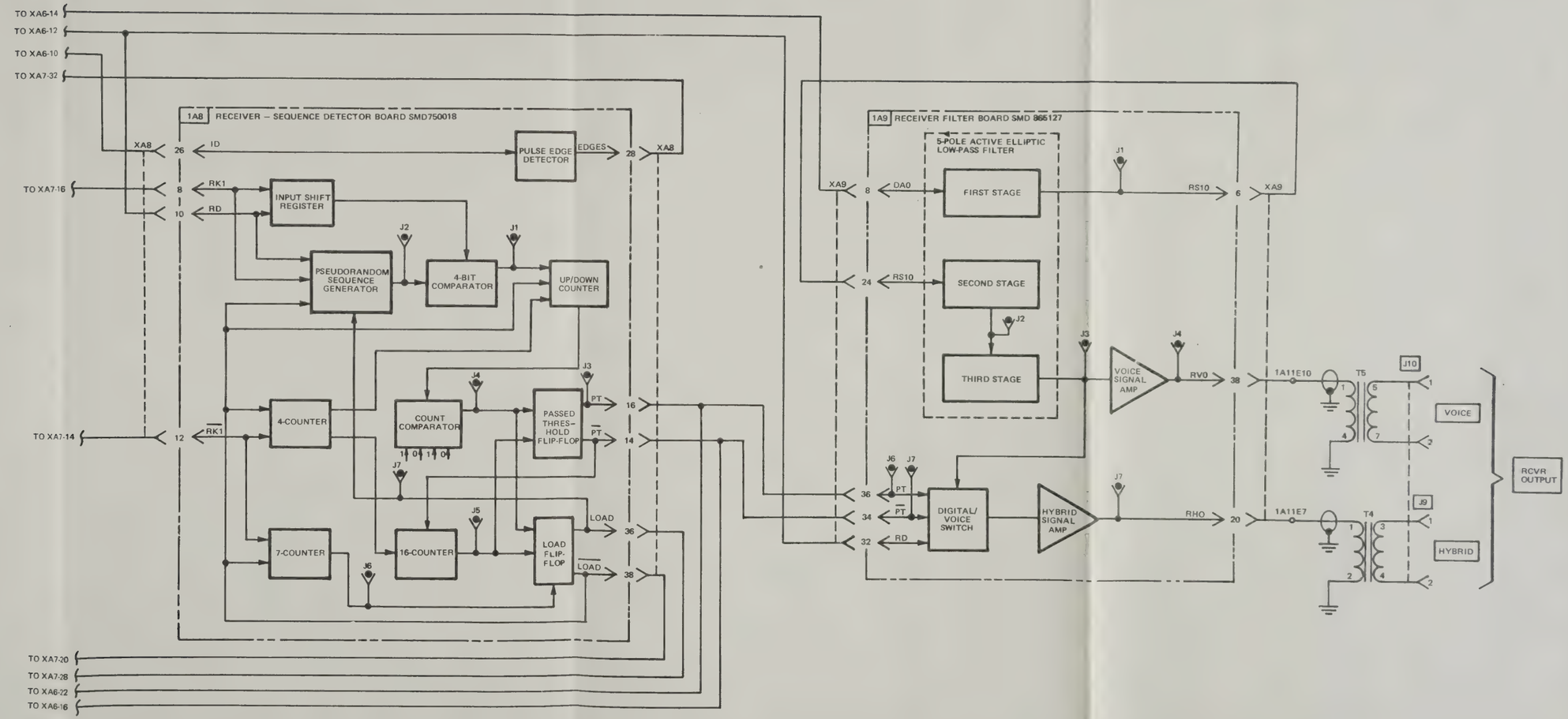


Figure FO-3 ②. Receiver functional diagram (sheet 2 of 2).

ELOVY031

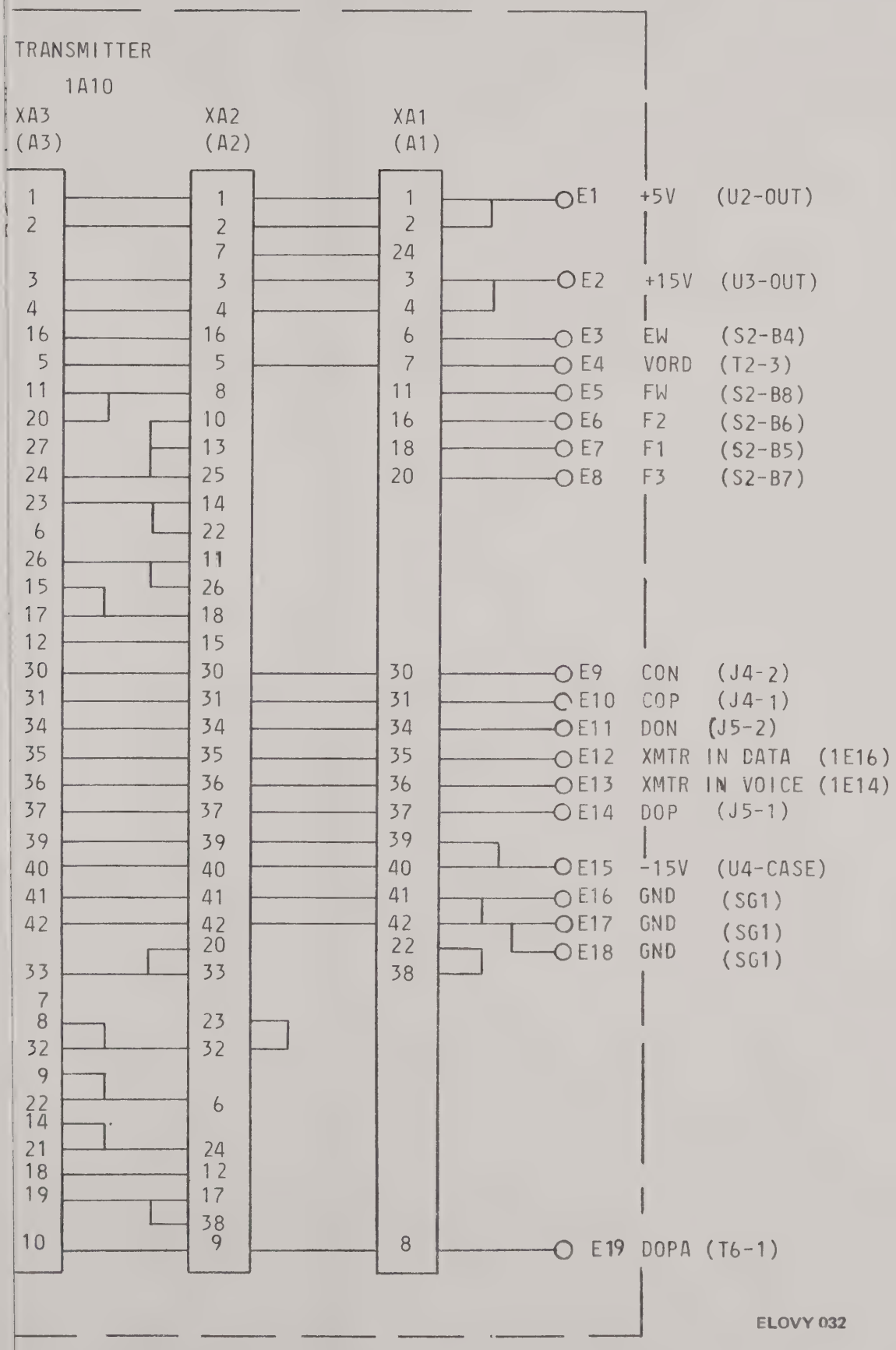


Figure FO-4. Chassis, interconnection of printed wiring board connectors.

NOTES:

1. TERMINALS E1 THROUGH E19 IN THE TRANSMITTER SECTION AND E1 THROUGH E16 IN THE RECEIVER SECTION ARE MOUNTED ON CONNECTOR MOUNTING ASSEMBLIES 1A10 AND 1A11 RESPECTIVELY.
2. REFERENCE DESIGNATIONS IN PARENTHESES ARE FOR PRINTED WIRING BOARDS MATING WITH RESPECTIVE RECEPTACLE CONNECTOR.

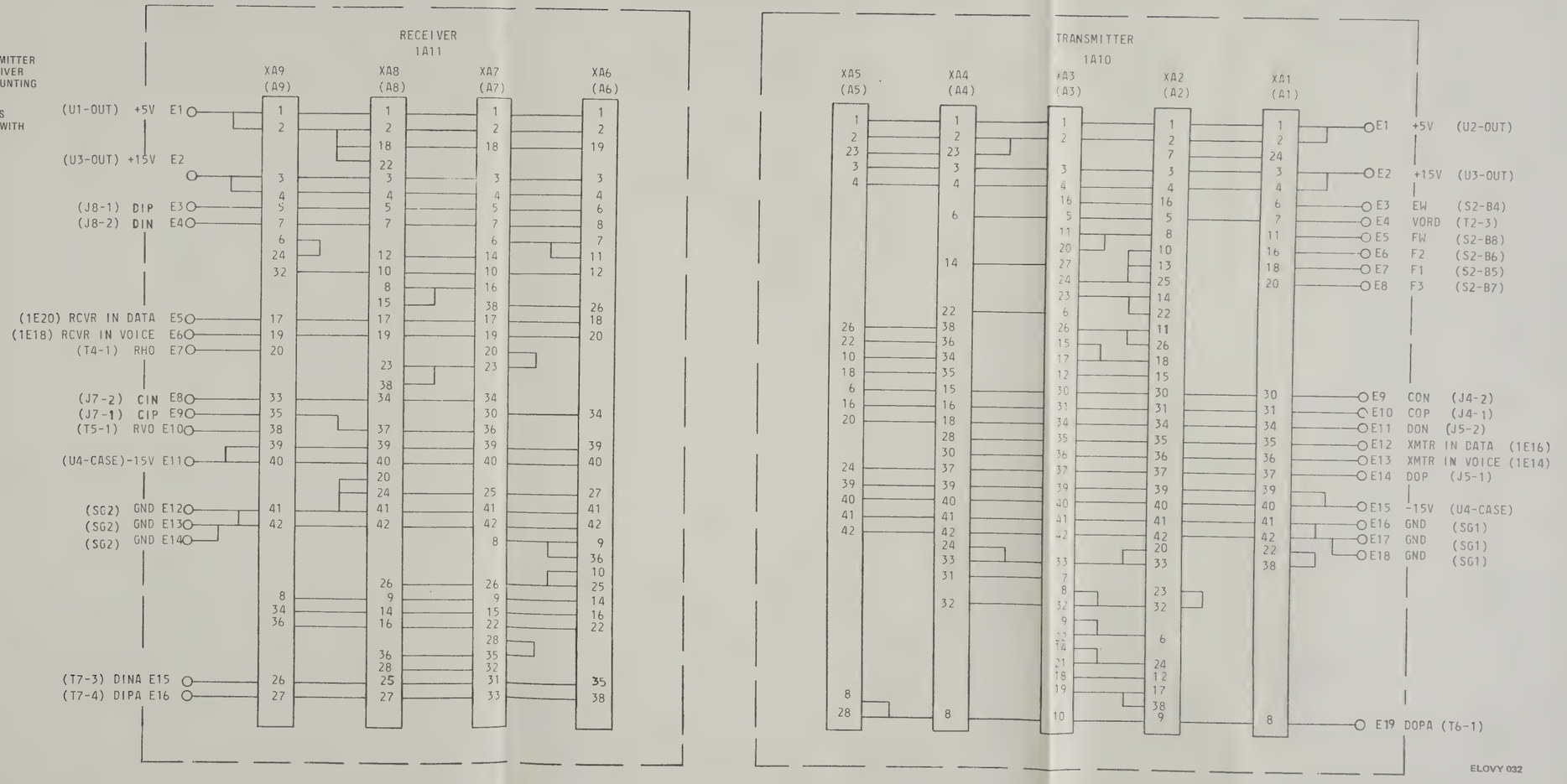


Figure FO-4. Chassis, interconnection of printed wiring board connectors.

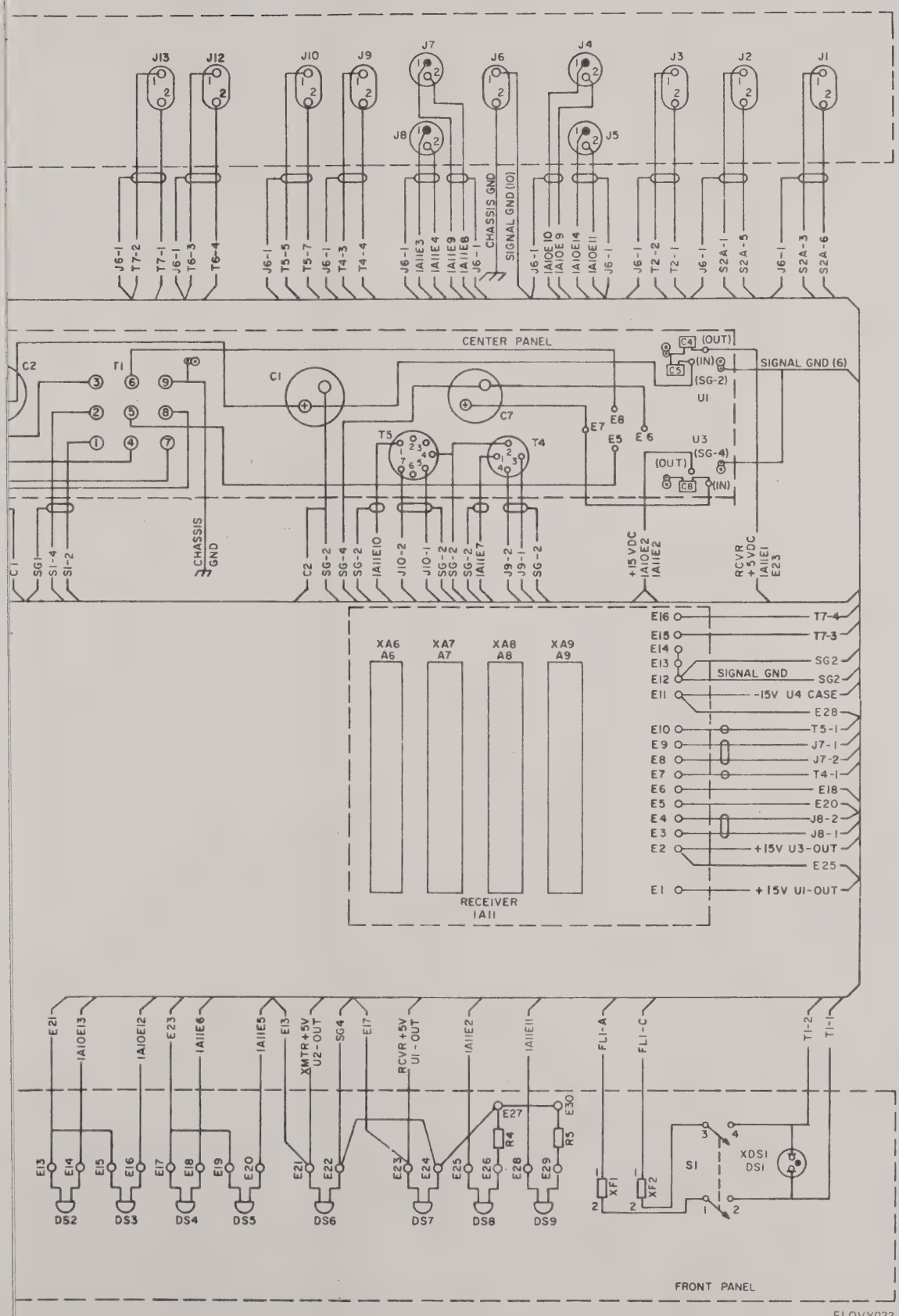
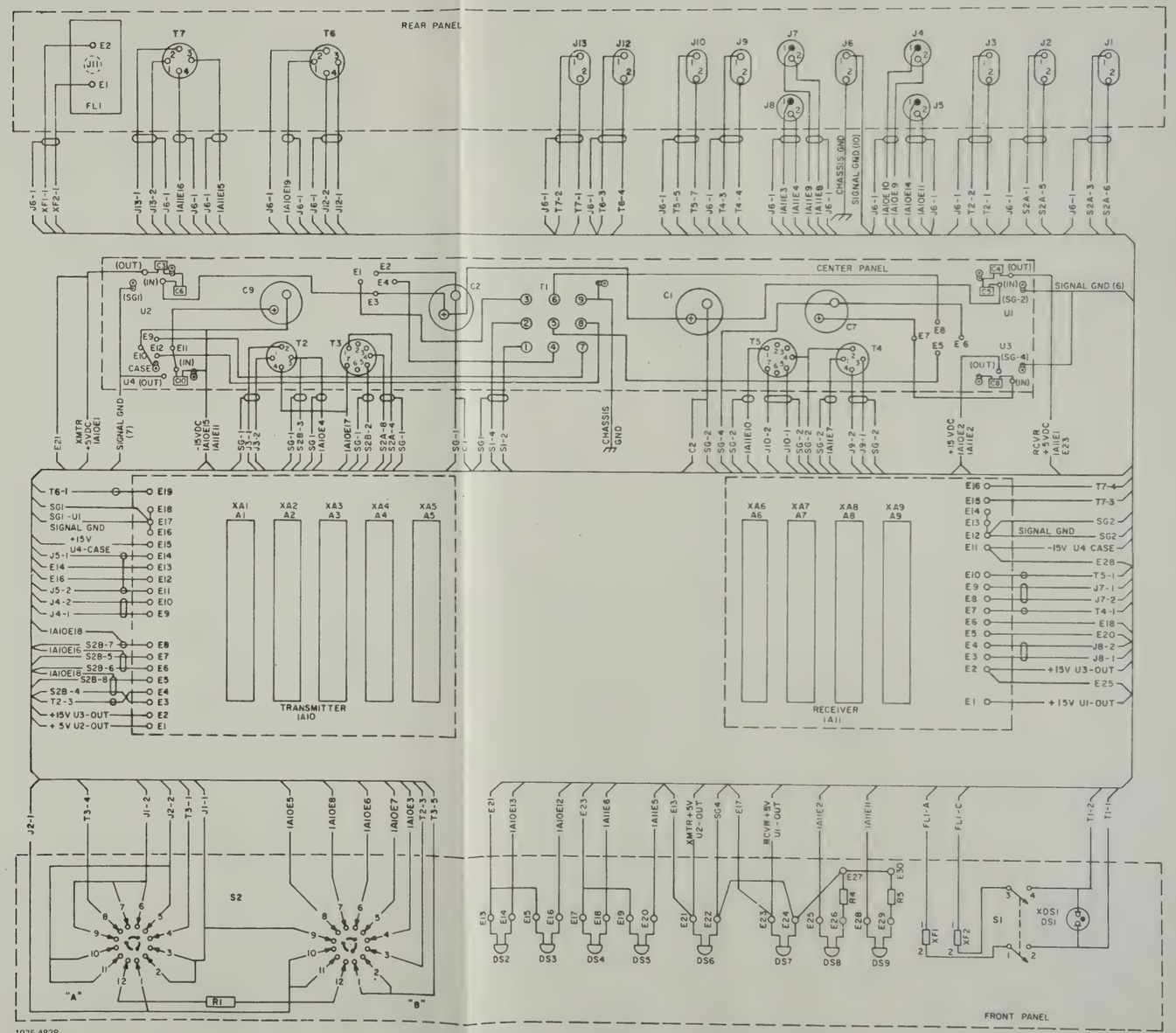


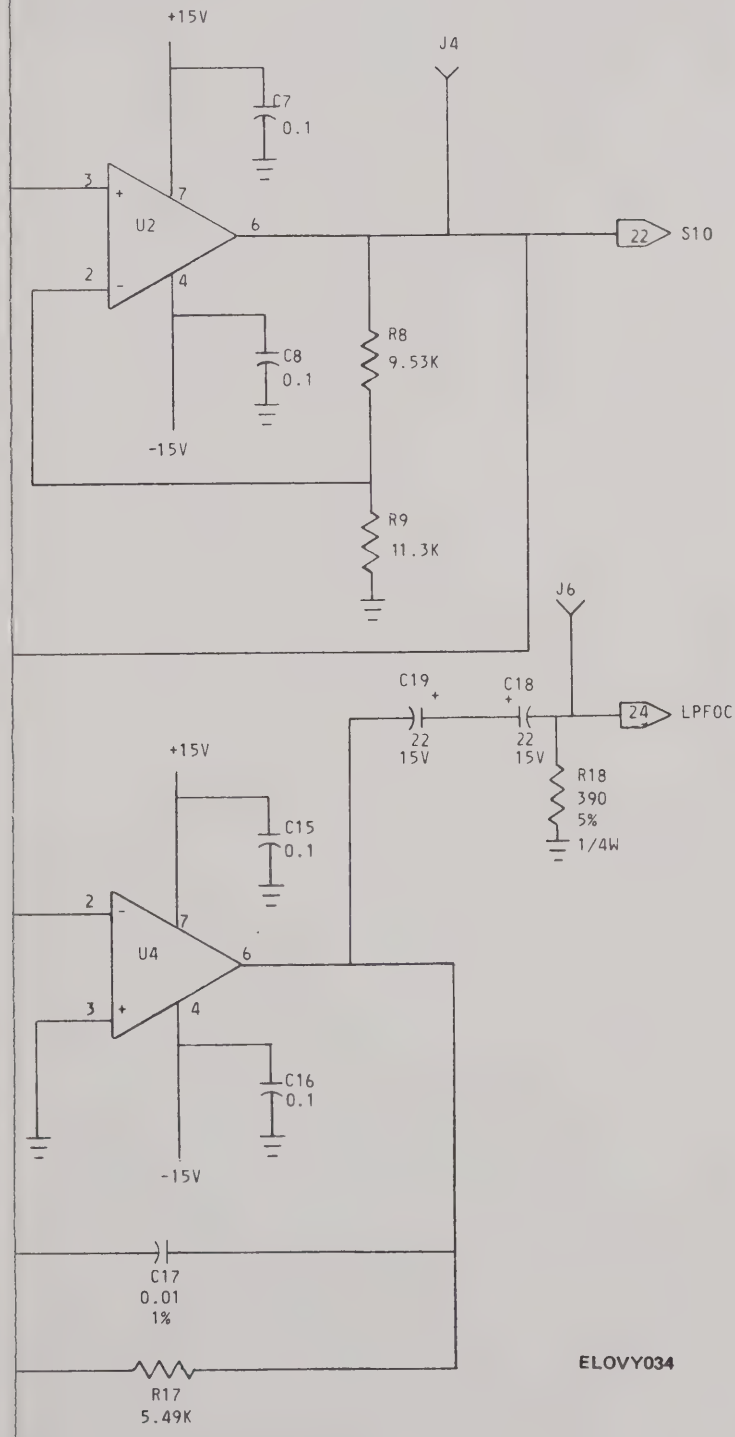
Figure FO-5. Interconnecting wiring diagram.



1075-4838
UNCLASSIFIED

Figure FO-5. Interconnecting wiring diagram.

ELOVY033



filter board 1A2 schematic diagram.

NOTES:

1. UNLESS OTHERWISE INDICATED, ALL: RESISTOR VALUES ARE IN OHMS, ±5%, 1/8 W. CAPACITOR VALUES ARE IN MICROFARADS.
2. ▷ INDICATES CONNECTOR PIN OF P1.
3. U1, U2, U3, U4 ARE PART NUMBER M38510/101-01BGA (U7B7741393).
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A1.

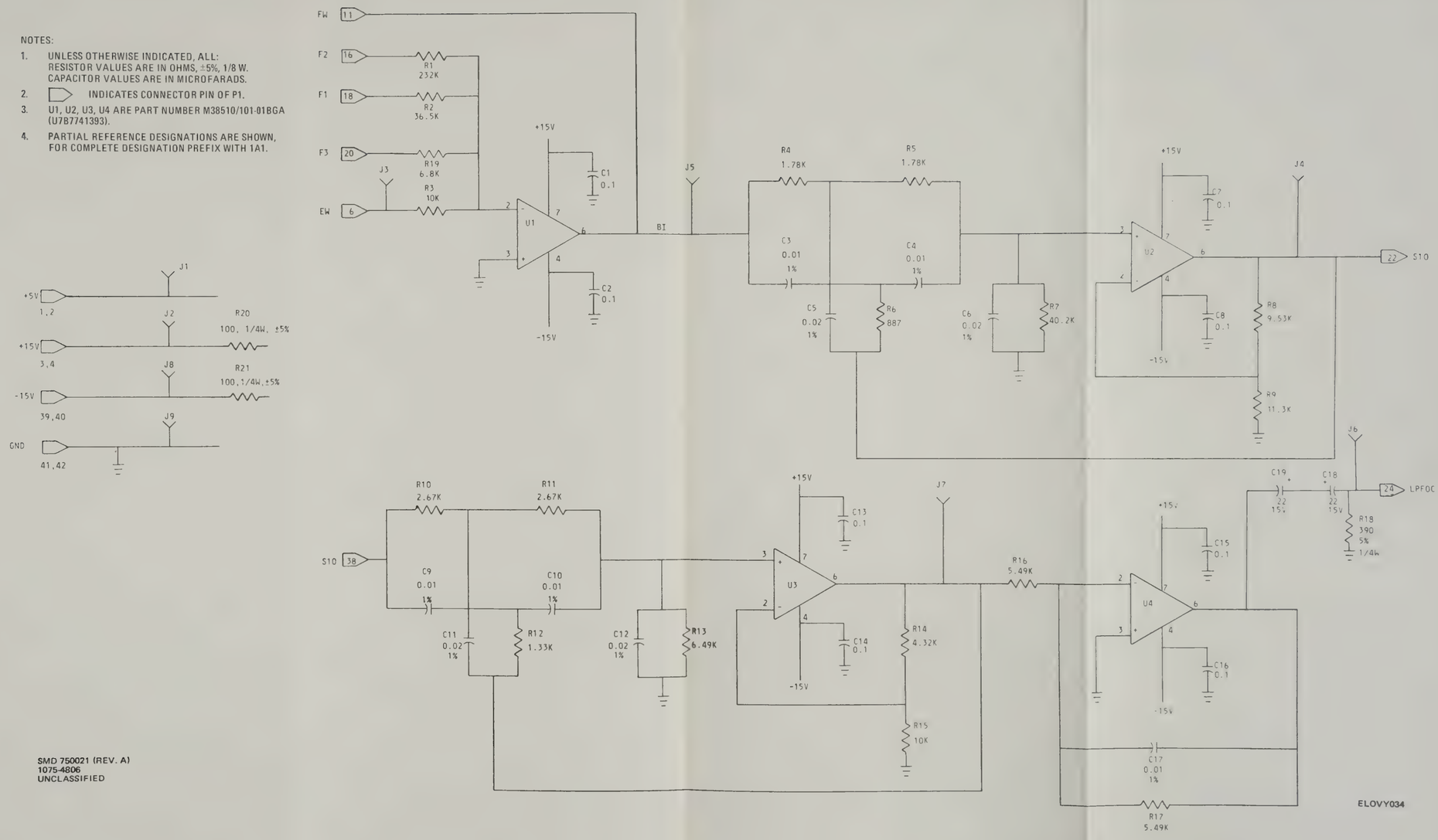
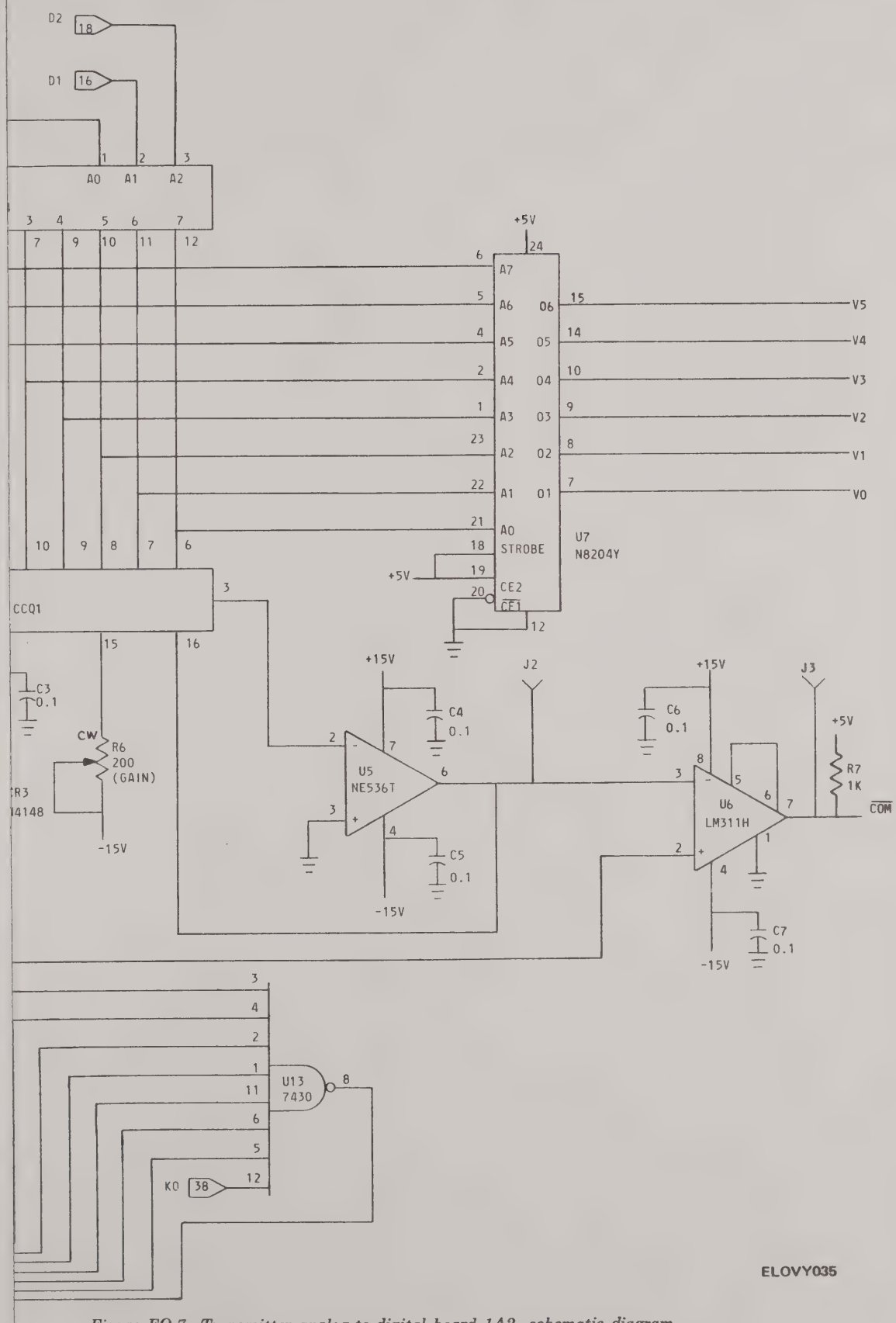


Figure FO-6. Transmitter filter board 1A2 schematic diagram.



ELOVY035

Figure FO-7. Transmitter analog-to-digital board 1A2, schematic diagram.

NOTES:

1. UNLESS OTHERWISE INDICATED, ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W. CAPACITOR VALUES ARE IN MICROFARADS.
2. ▷ INDICATES CONNECTOR PIN OF P1.
3. PARTIAL REFERENCE DESIGNATION ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A2.

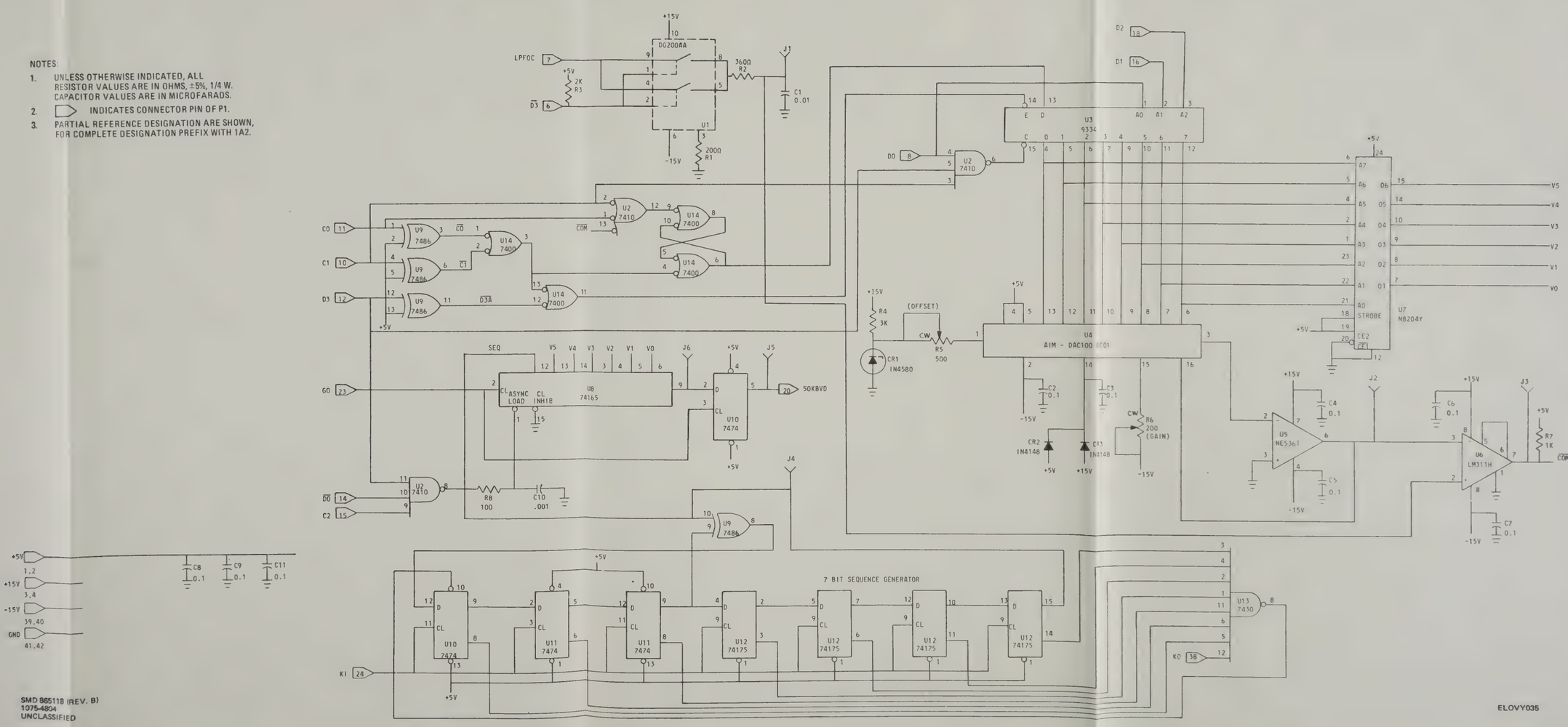


Figure FO-7. Transmitter analog-to-digital board 1A2, schematic diagram.

ELOVY035

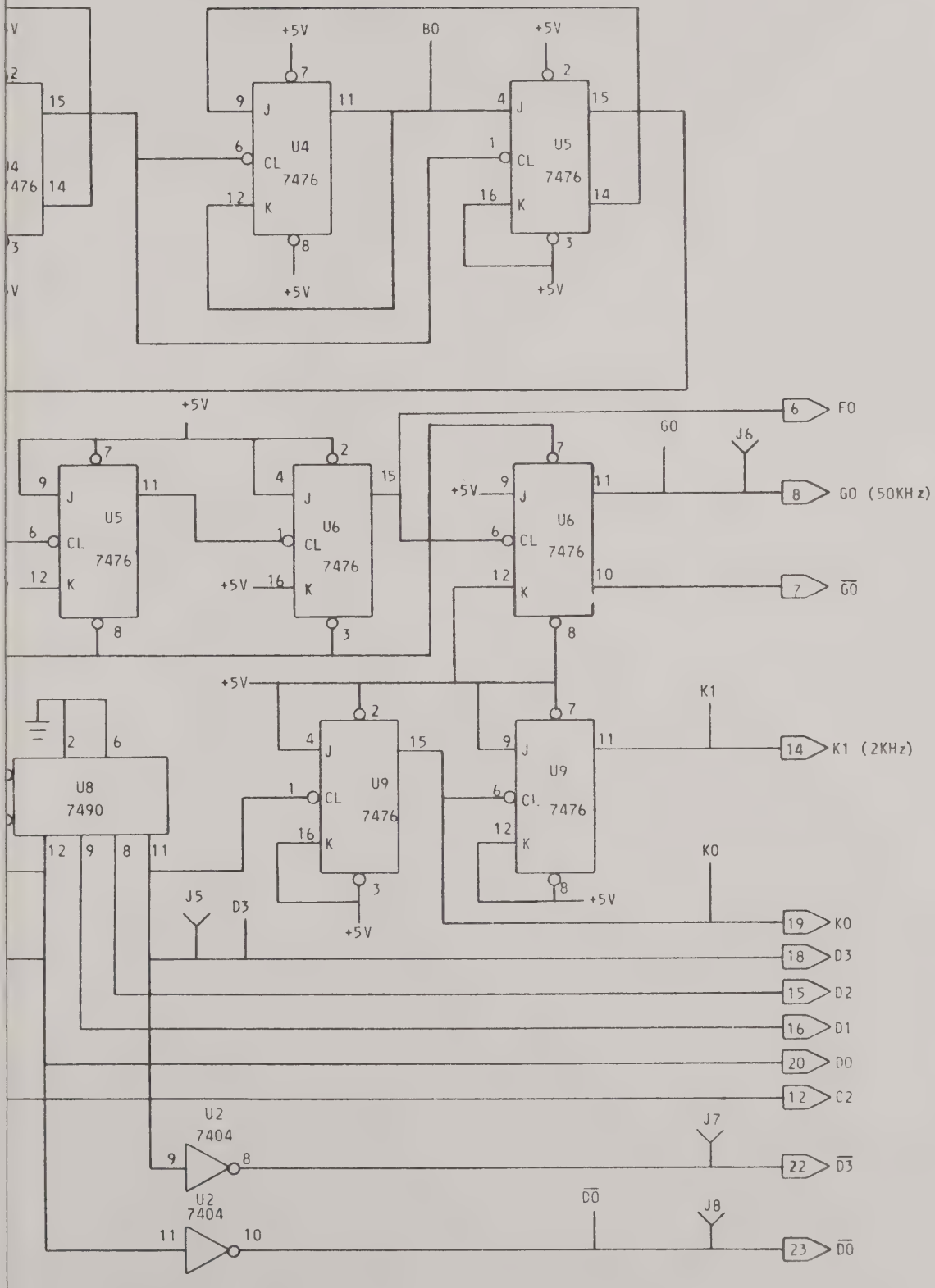


Figure FO-8. Transmitter timing board 1A3, schematic diagram.

ELOVY036

NOTES:

1. UNLESS OTHERWISE INDICATED, ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W. CAPACITOR VALUES ARE IN MICROFARADS.
2. ▷ INDICATES CONNECTOR PIN OF P1.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A3.

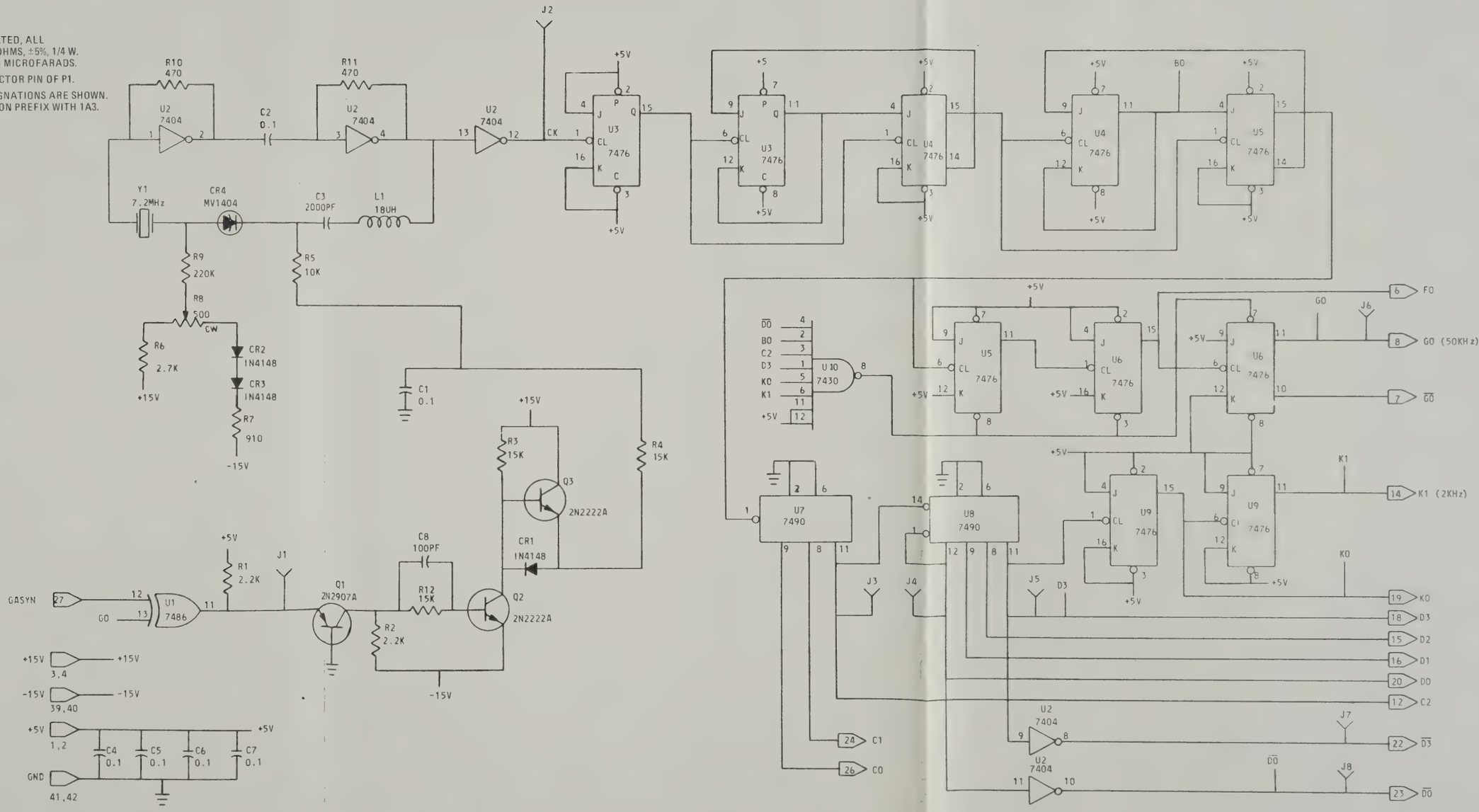


Figure FO-8. Transmitter timing board 1A3, schematic diagram.

ELOVY036

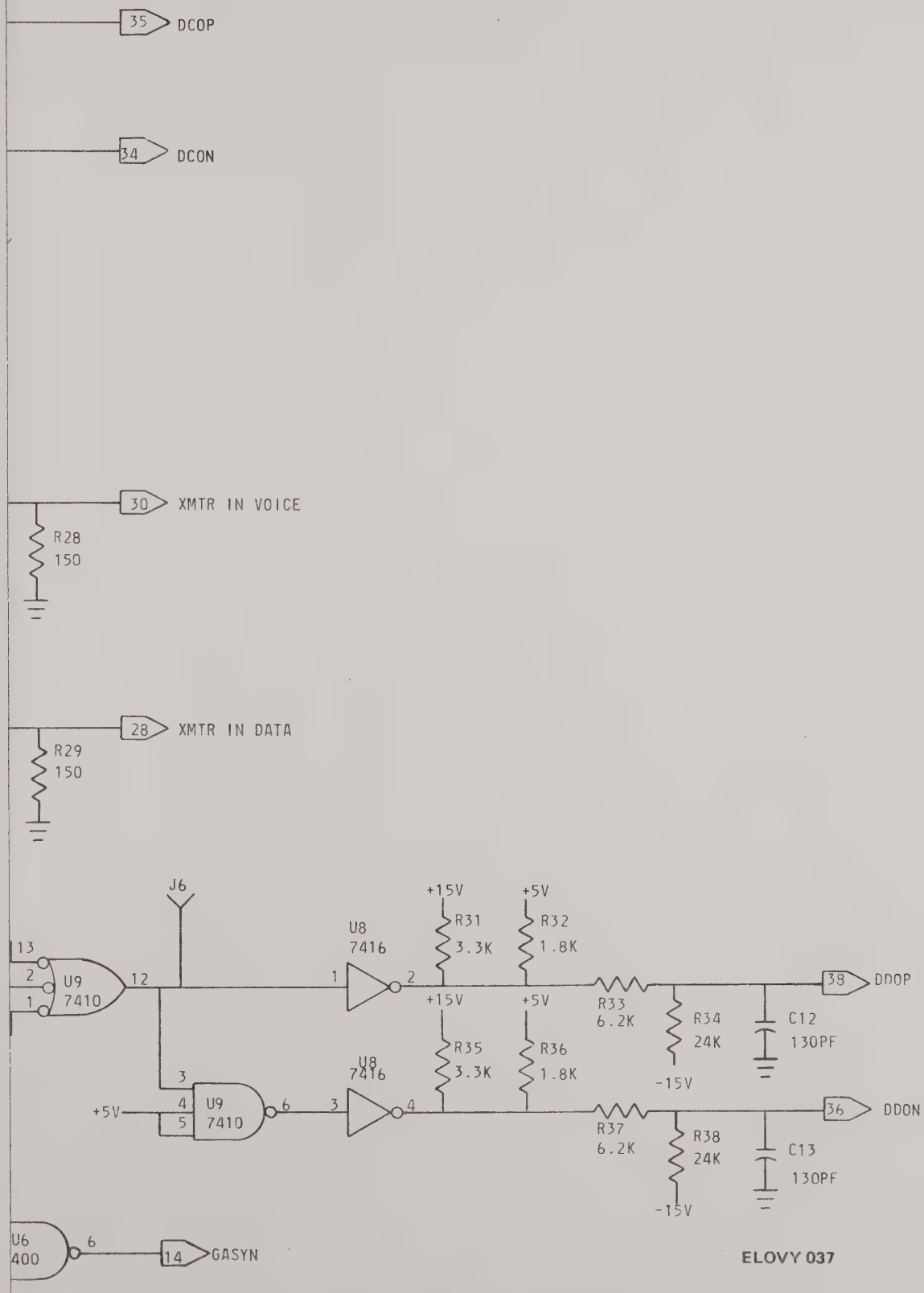


Figure FO-9. Transmitter data presence board 1A4, schematic diagram.

NOTES:

1. UNLESS OTHERWISE INDICATED, ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W. CAPACITOR VALUES ARE IN MICROFARADS.
2. INDICATES CONNECTOR PIN OF P1.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A4.

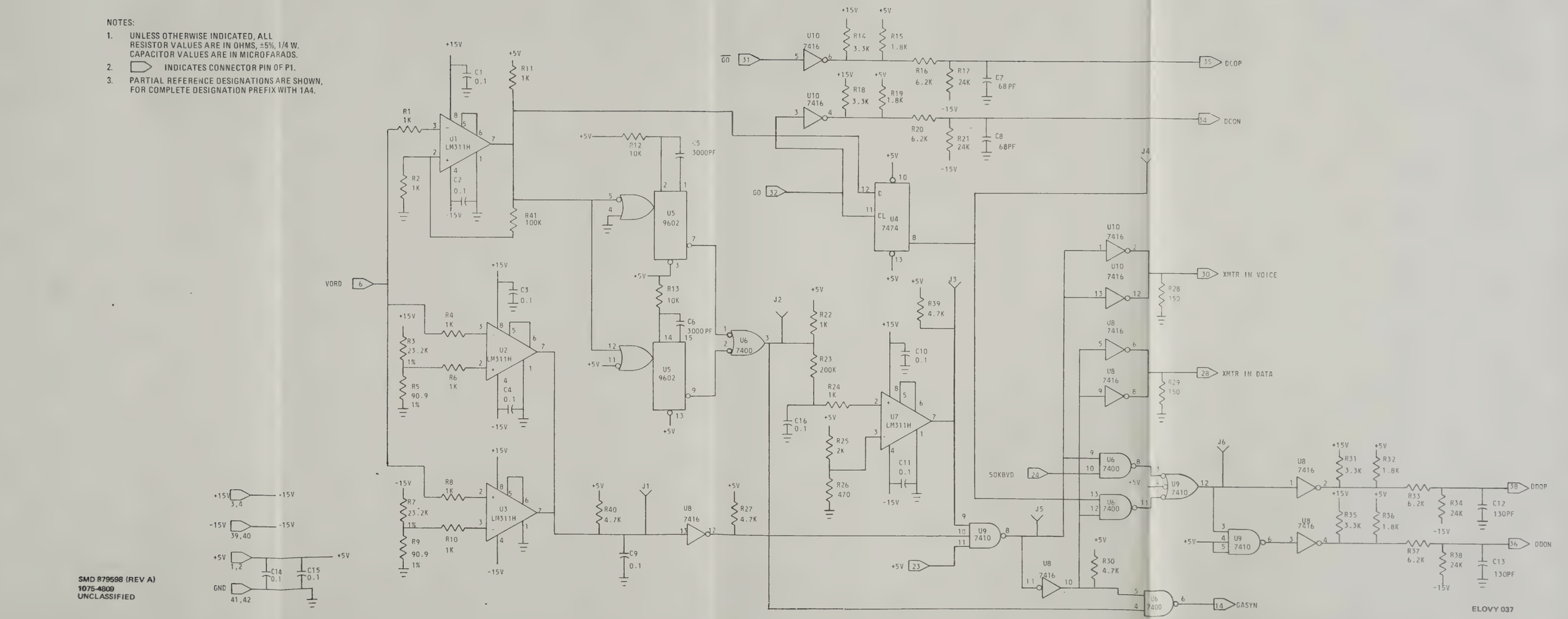


Figure FO-9. Transmitter data presence board 1A4, schematic diagram.

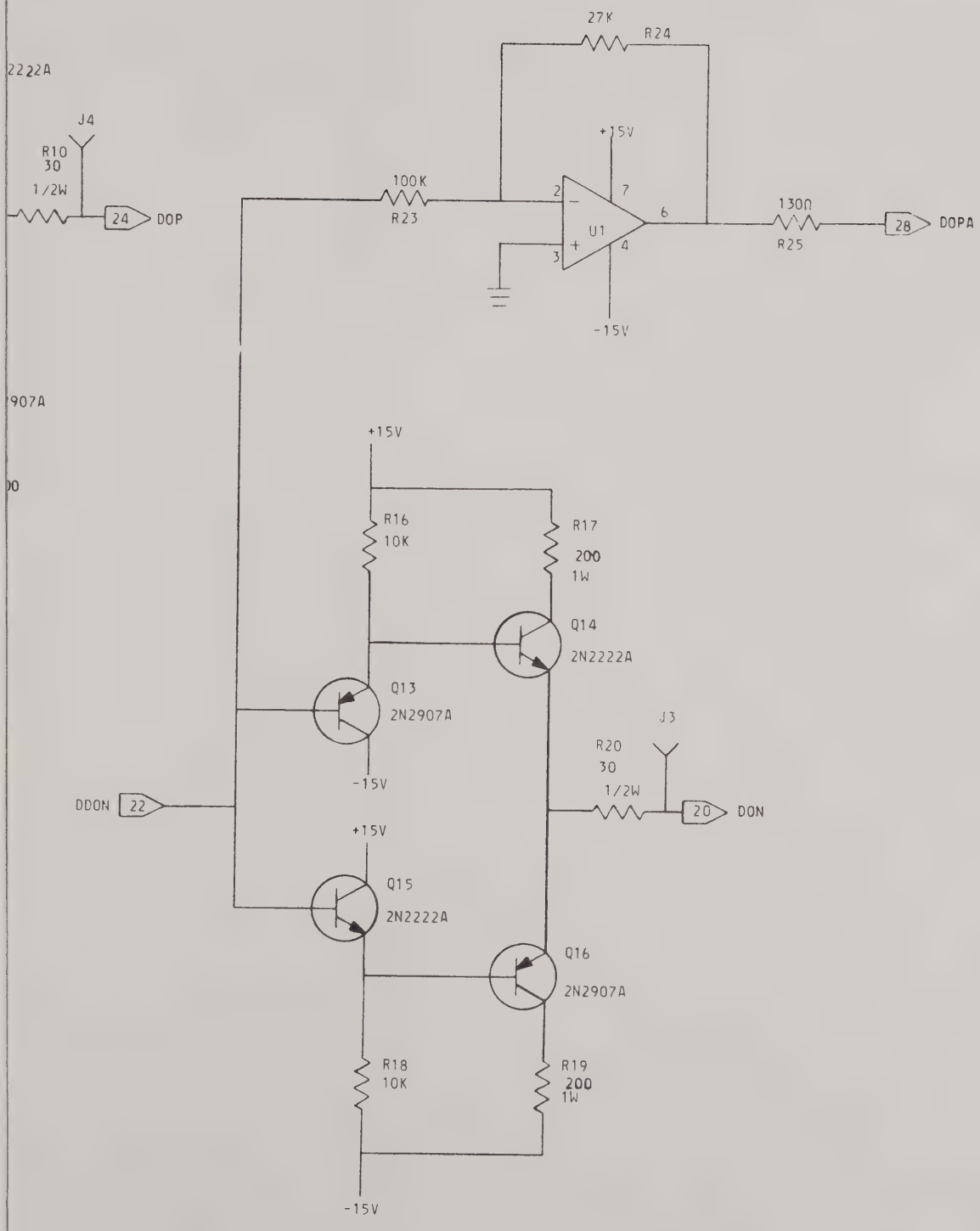


Figure FO-10. Transmitter interface board 1A5, schematic diagram.

ELOVY038

NOTES:

1. UNLESS OTHERWISE INDICATED, ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W. CAPACITOR VALUES ARE IN MICROFARADS.
2. ⇨ INDICATES CONNECTOR PIN OF P1.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A5.
4. U1 IS PART NUMBER M38510/101-01BGA.

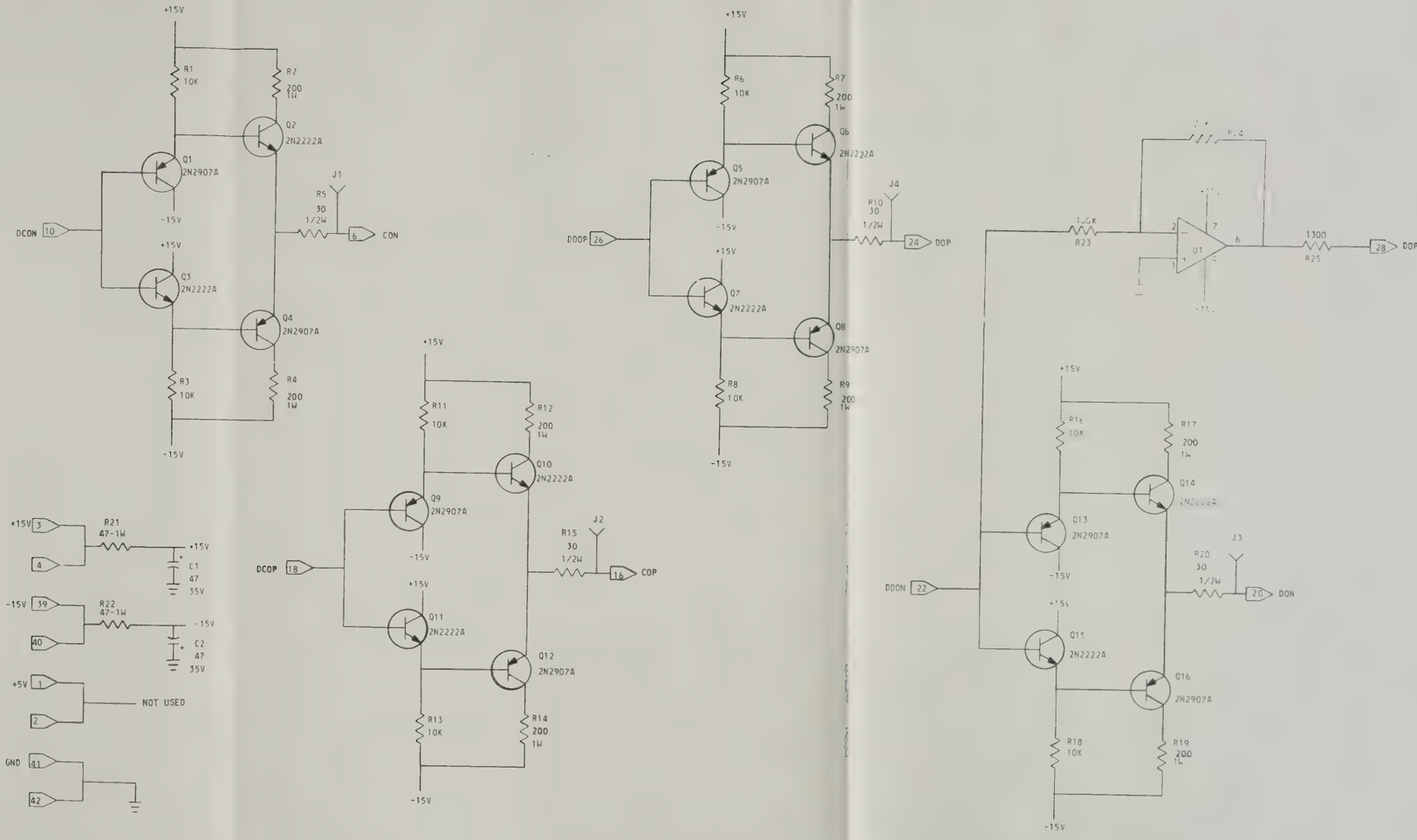
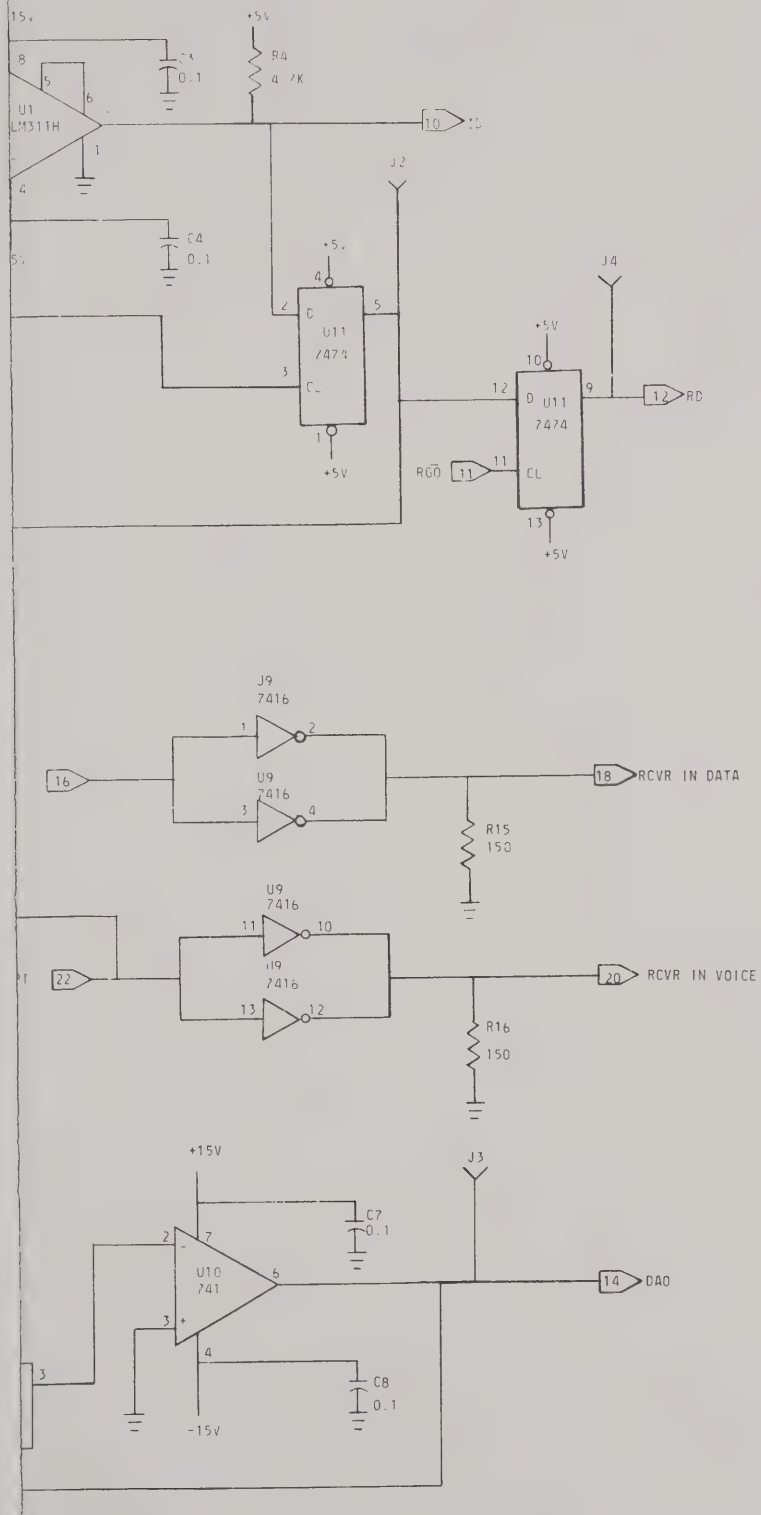


Figure FO-10. Transmitter interface board 1A5, schematic diagram.

ELOVY038



al-to-analog board 1A6, schematic diagram.

ELOVY039

NOTES:

1. UNLESS OTHERWISE INDICATED, ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W. CAPACITOR VALUES ARE IN MICROFARADS.
2. ⬠ INDICATES CONNECTOR PIN OF P1.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A6.

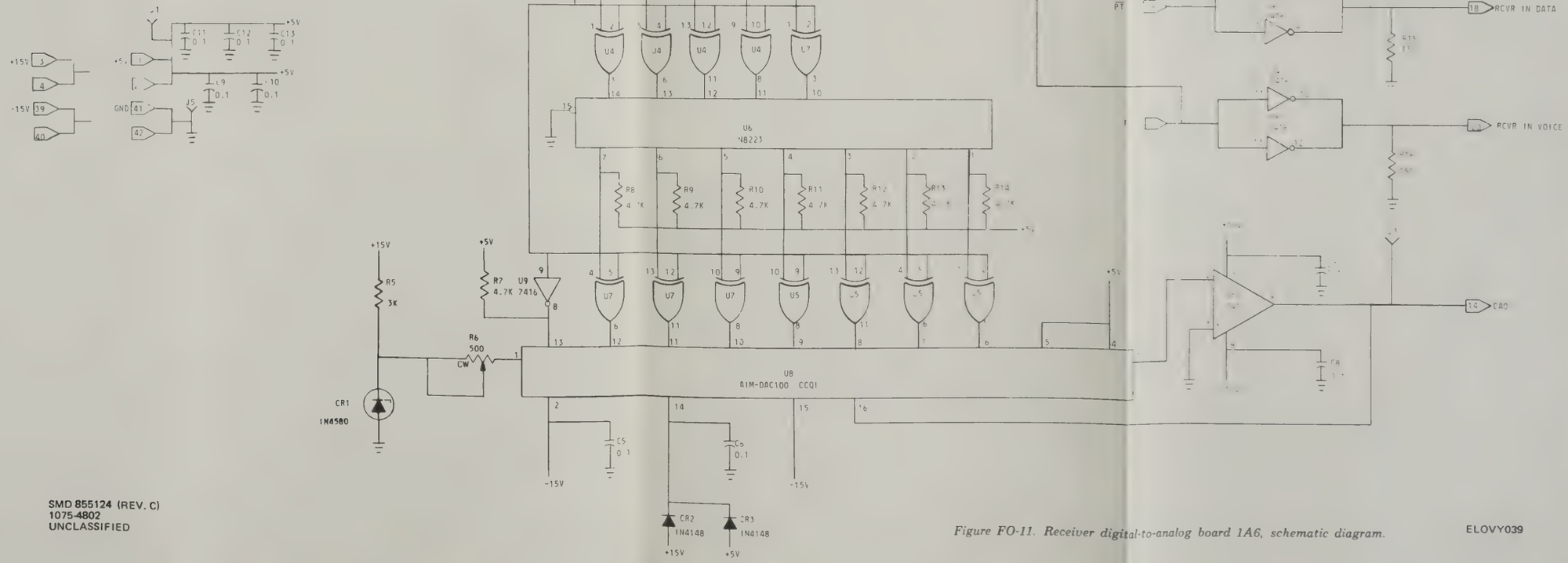
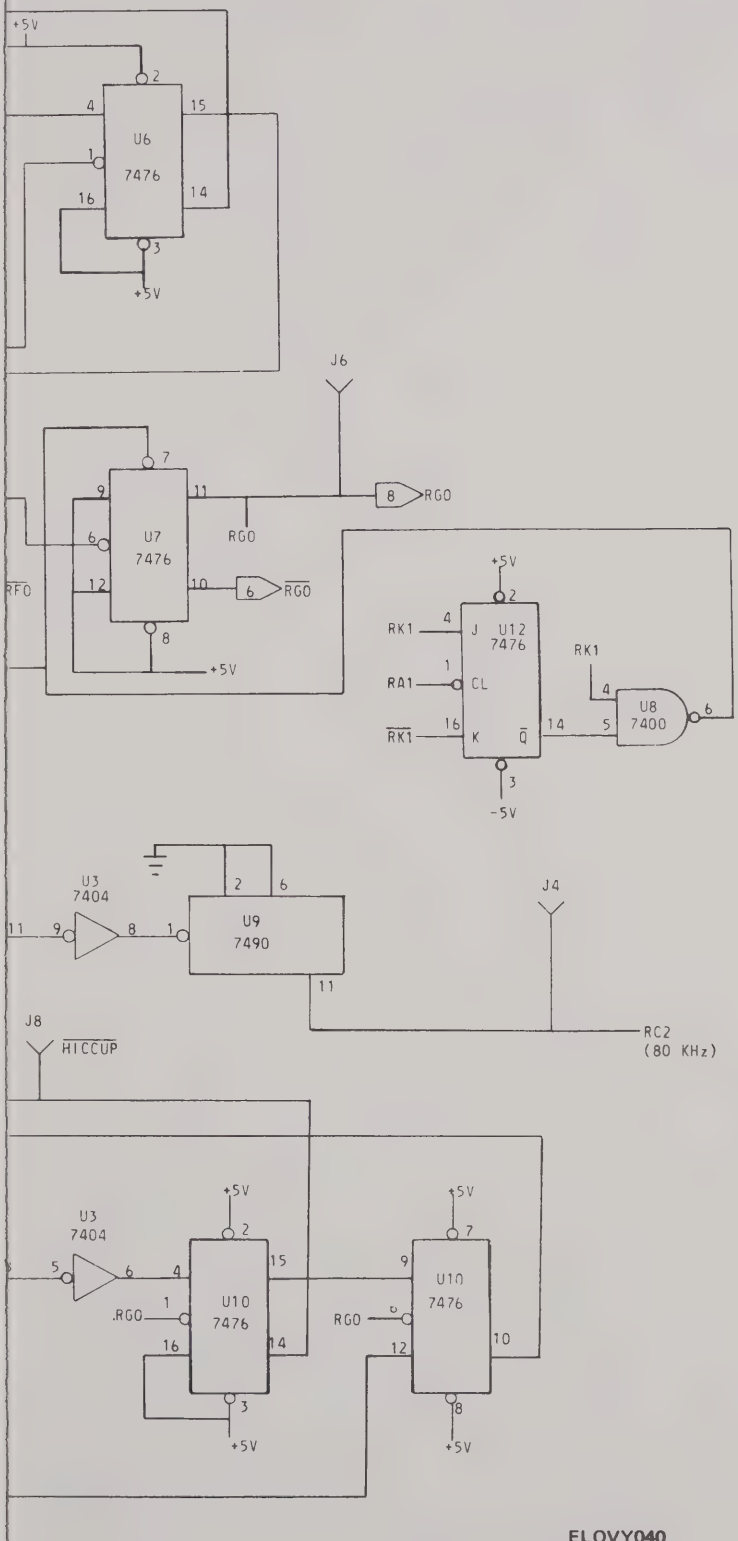


Figure FO-11. Receiver digital-to-analog board 1A6, schematic diagram.

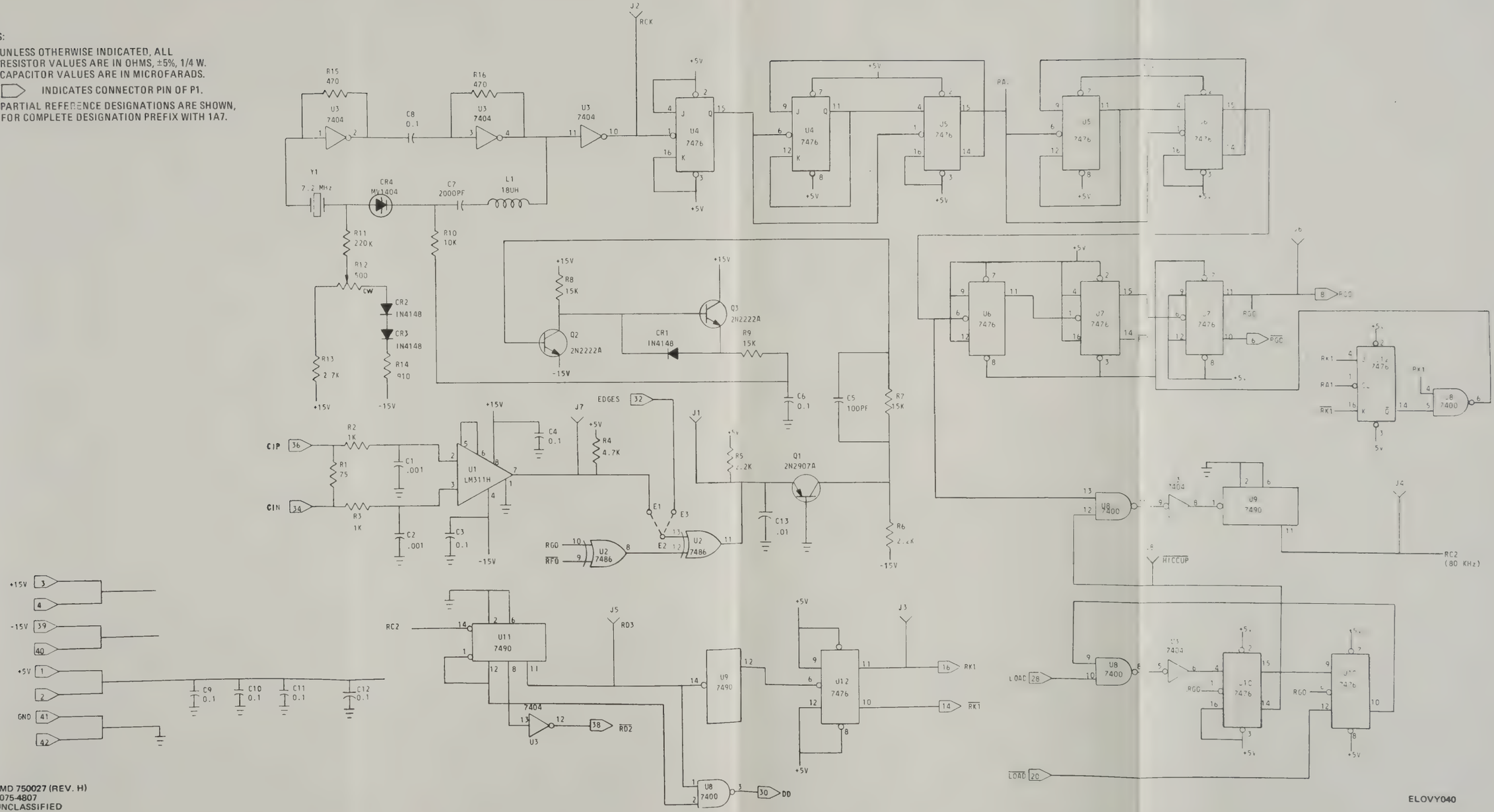
ELOVY039



iming board 1A7, schematic diagram.

NOTES:

1. UNLESS OTHERWISE INDICATED, ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W. CAPACITOR VALUES ARE IN MICROFARADS.
2. ⇨ INDICATES CONNECTOR PIN OF P1.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A7.



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ELOVY040

Figure FO-12. Receiver timing board 1A7, schematic diagram.

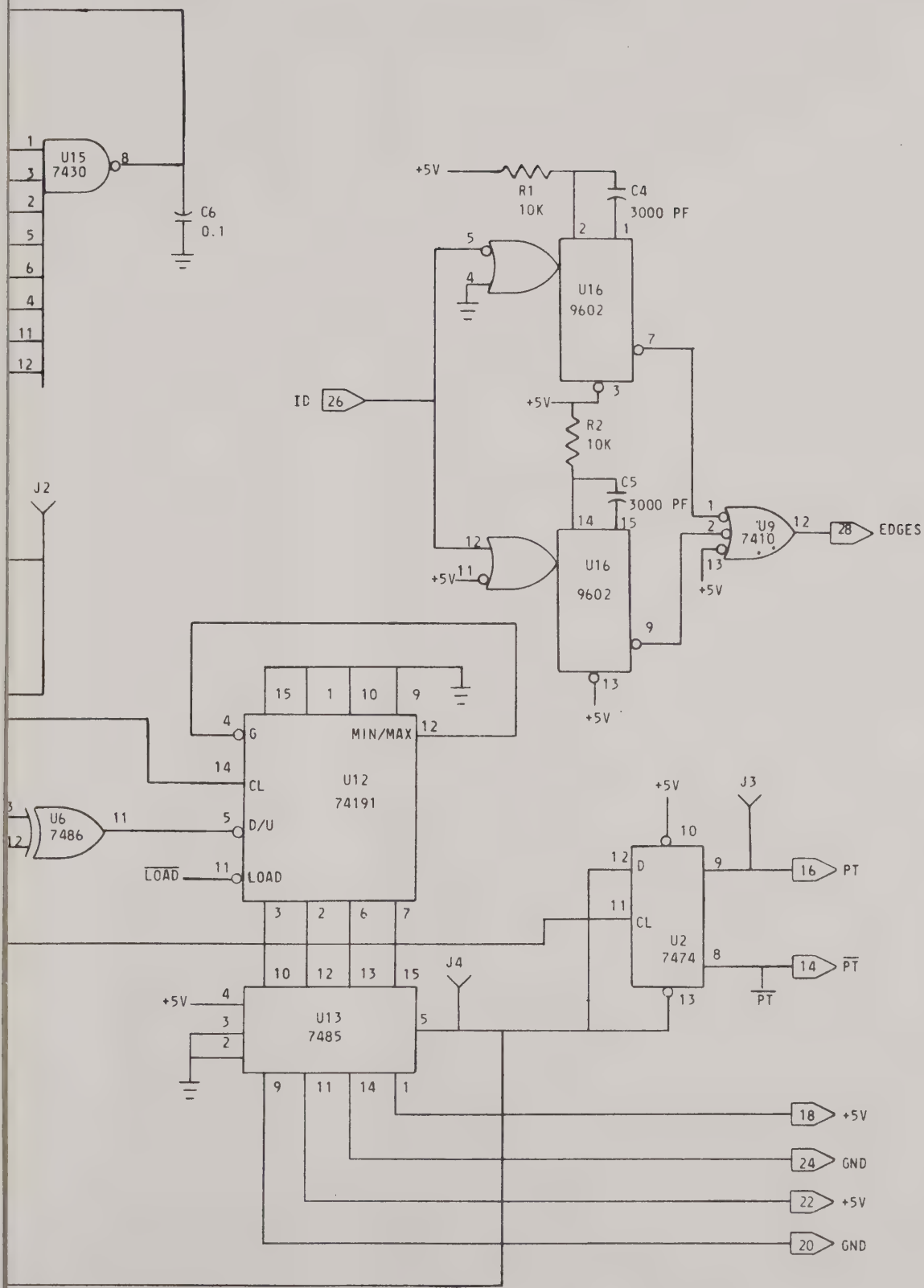


Figure FO-13. Receiver sequence detector board 1A8, schematic diagram. ELOVY041

NOTES:

1. UNLESS OTHERWISE INDICATED, ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W. CAPACITOR VALUES ARE IN MICROFARADS.
2. ▷ INDICATES CONNECTOR PIN OF P1.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A8.

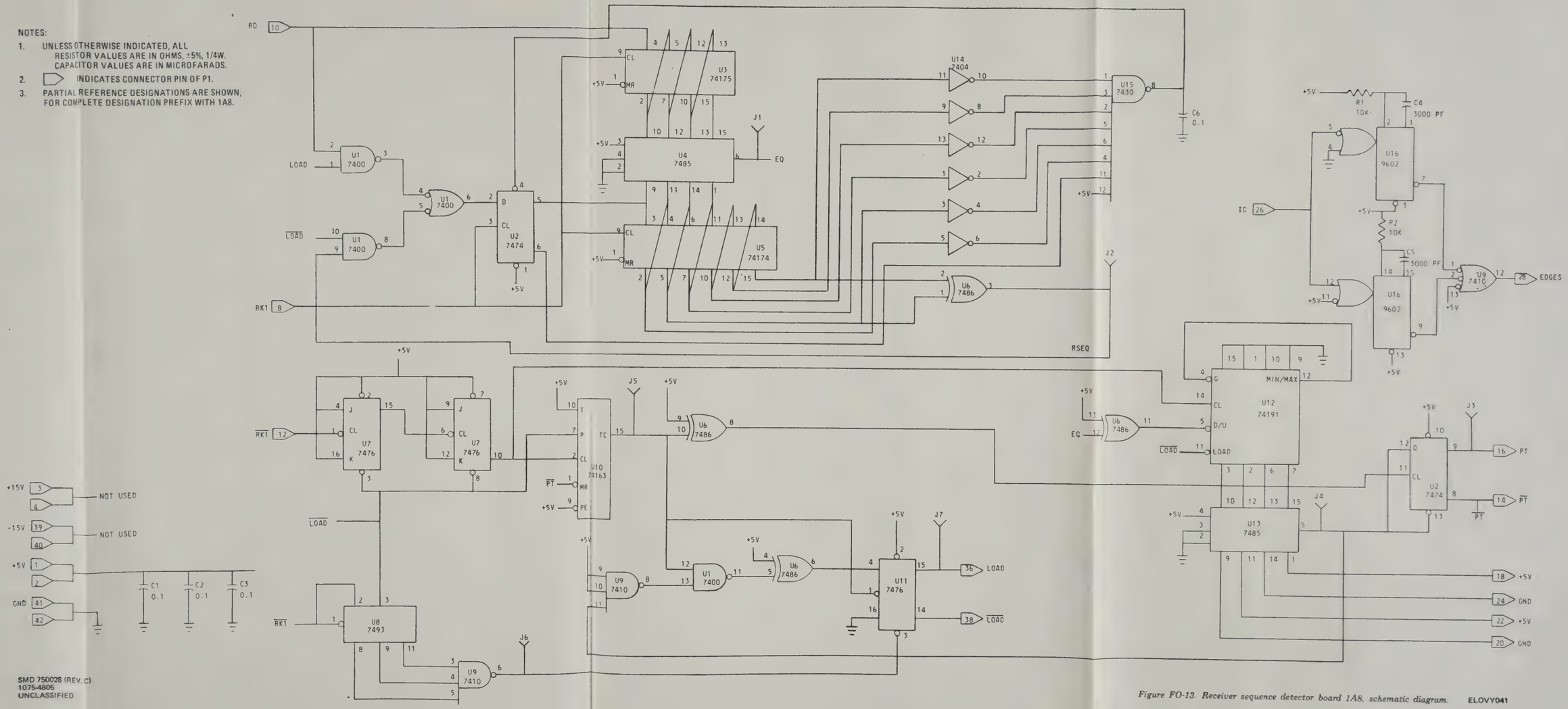


Figure FO-13. Receiver sequence detector board 1A8, schematic diagram. ELOVY041

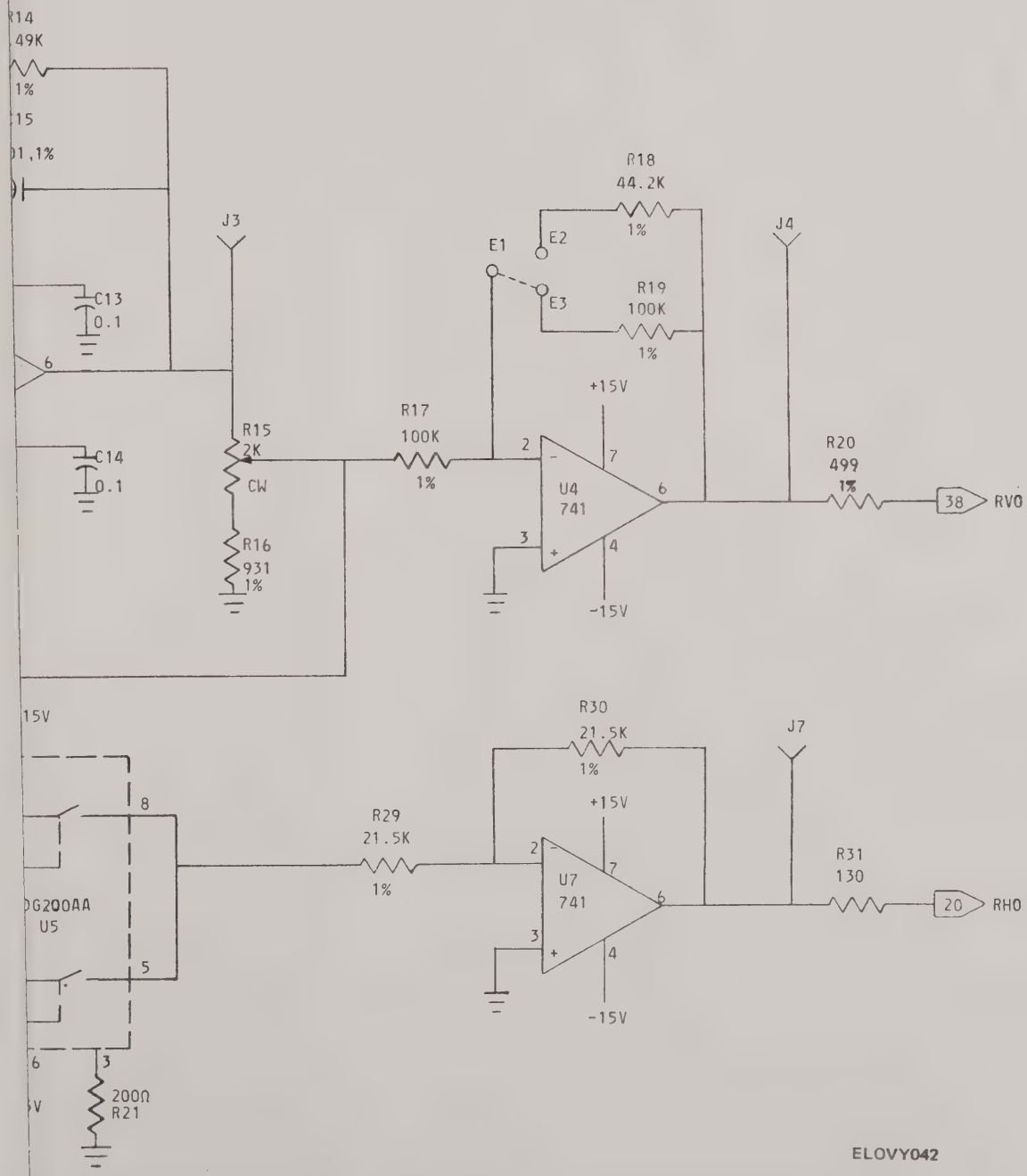


Figure FO-14. Receiver filter board 1A9, schematic diagram.

NOTES:

1. UNLESS OTHERWISE INDICATED, ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W. CAPACITOR VALUES ARE IN MICROFARADS.
2. ⇨ INDICATES CONNECTOR PIN OF P1.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A9.

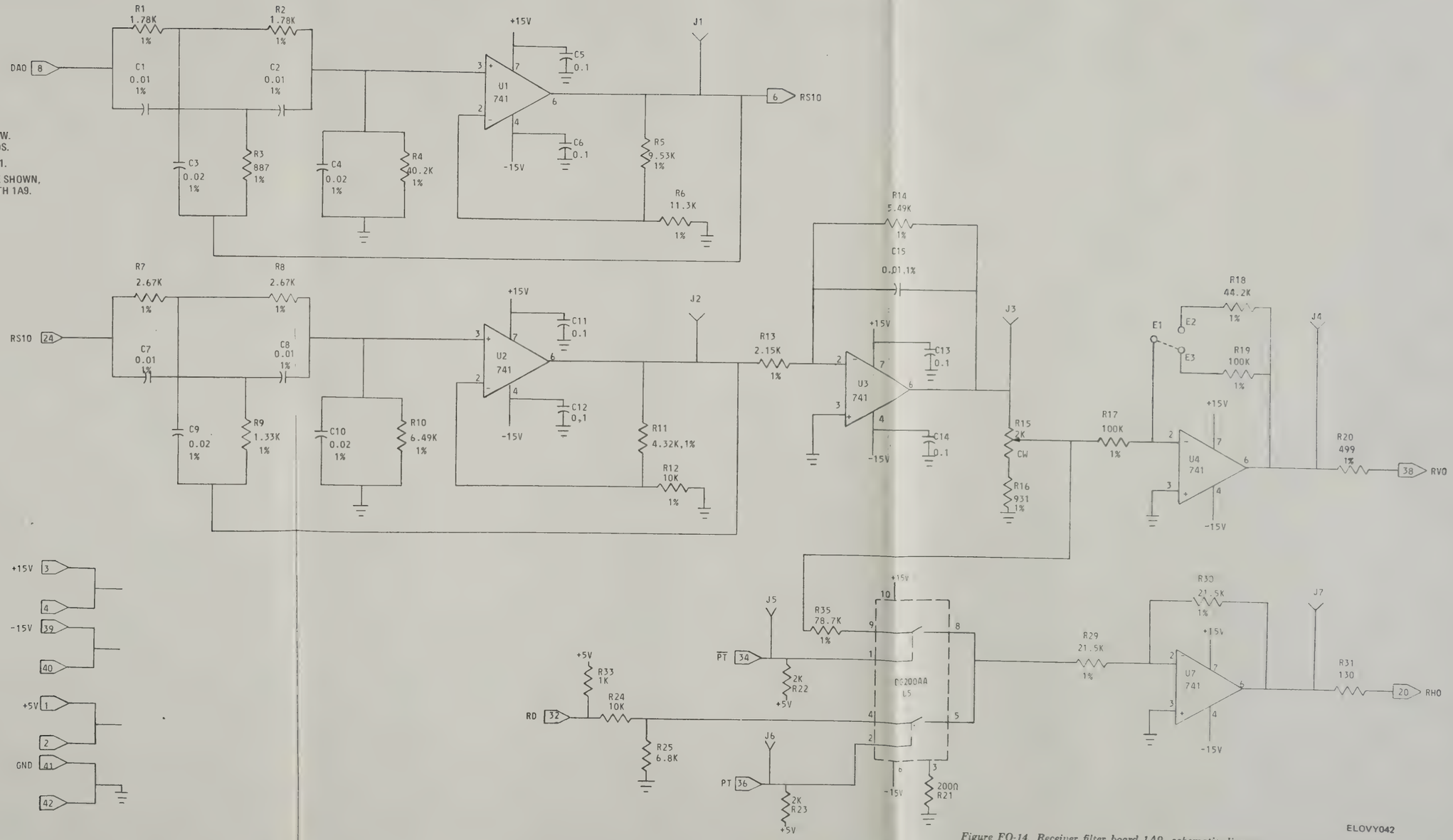


Figure FO-14. Receiver filter board 1A9, schematic diagram.

ELOVY042

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM, CY CB	0	0	1			±20%	±20%		A			-55°$_{TO}$+70°C	10-55 Hz
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55°$_{TO}$+85°C	
ORANGE		3	3	1,000		±30%			D		D	300		
YELLOW		4	4	10,000					E				-55°$_{TO}$+125°C	10-2,000Hz
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55°$_{TO}$+150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						

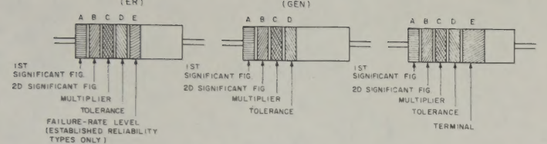
TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS. MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

Figure FO-15. Color code markings for MIL STD resistors, inductors, and capacitors.



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS AND INDICATES TYPE OF TERMINAL.

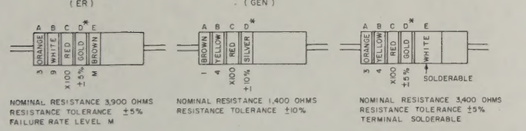
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED.)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

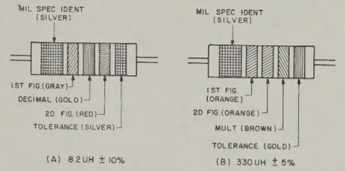
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS.



(A) 8.2UH ±10% (B) 330UH ±5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED.

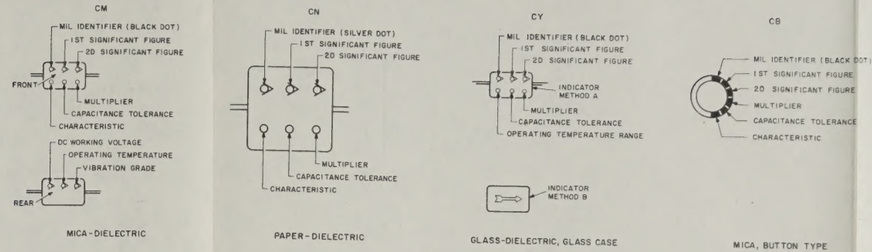
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.

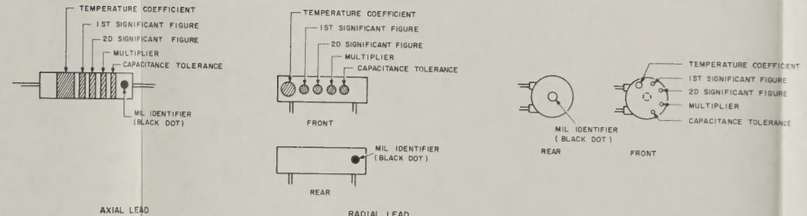


MICA-DIELECTRIC

PAPER-DIELECTRIC

GLASS-DIELECTRIC, GLASS CASE

MICA, BUTTON TYPE



AXIAL LEAD

RADIAL LEAD

DISK-TYPE

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER	CAPACITANCE TOLERANCE				CHARACTERISTIC			DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM, CY, CB	0	0	1			±20%	±20%		A			-55°C TO +70°C	10-55 HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55°C TO +85°C	
ORANGE		3	3	1,000		±30%			D		D	300		
YELLOW		4	4	10,000					E				-55°C TO +125°C	10-2,000HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55°C TO +150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT*	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER†	CAPACITANCE TOLERANCE		MIL ID.
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	−30	1	1	10	±1%		
RED	−80	2	2	100	±2%	±0.25 UUF	
ORANGE	−150	3	3	1,000			
YELLOW	−220	4	4				
GREEN	−330	5	5		±5%	±0.5 UUF	
BLUE	−470	6	6				
PURPLE (VIOLET)	−750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.
* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

Figure FO-15. Color code markings for MIL STD resistors, inductors, and capacitors.

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